









Principles: Qua	C🚧 PairEnt	
Quantum Bit	$ \psi\rangle = a 0\rangle + b 1\rangle$	-al
Multiple QuBits	$\left \psi\right\rangle = \left \psi\right\rangle_1 \otimes \left \psi\right\rangle_2$	
$ \psi\rangle = a 00\rangle + b 01$		
f is a quantum ga	ite	
$a f(00)\rangle + b f(01)\rangle$	$+ c f(10)\rangle + d f(11)\rangle$	0
Quantum parallelism: parallel evaluations grow exponentially with the number of Qubits (≈2 <sup>n</sup> )		
Quantum co	omputation	
Vandersypse	n, arXiv:0205193v1 (2002)	



















Requirements against <i>real</i> ReRAM devices			
<ul> <li>Write/erase voltage level:</li> <li>Write/erase times:</li> <li>Read-out voltage level:</li> <li>Read-out current level:</li> <li>OFF to ON resistance ratio</li> <li>OFF state resistances</li> </ul>	< 2 Volt < 100 ns < 1 Volt ~ 0.001 – 1 mA > 2 < 100 kΩ		
<ul> <li>Endurance</li> <li>Retention times</li> <li>Non-volatility also during read-</li> </ul>	<ul> <li>&gt; 10<sup>7</sup> writing cycles</li> <li>&gt; 10 years</li> <li>out operations R. Waser <i>et al.</i>, Adv. Mat. <b>21</b>, 2632 (2009).</li> </ul>		
	J. J. Yang et al., Nat. Nanotech. 8, 13 (2013).		
<ul> <li>CMOS competitive scaling</li> <li>CMOS compatible material systems and technology</li> </ul>			
A real resistive memory device must comply to ALL of the above requirements			
A highly non-linear voltage res	sponse function is essential		

























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