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NANOSENSORS
Centre for Energy Research
Institute of Technical Physics and Materials Science

ADVANCED SEMICONDUCTOR DEVICES

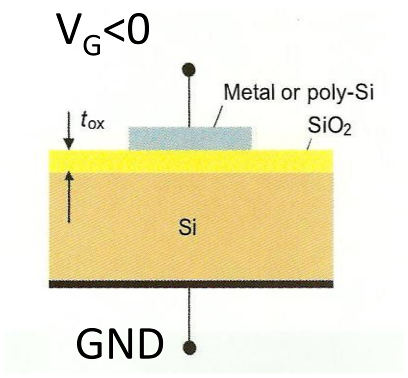
05_MOSFET

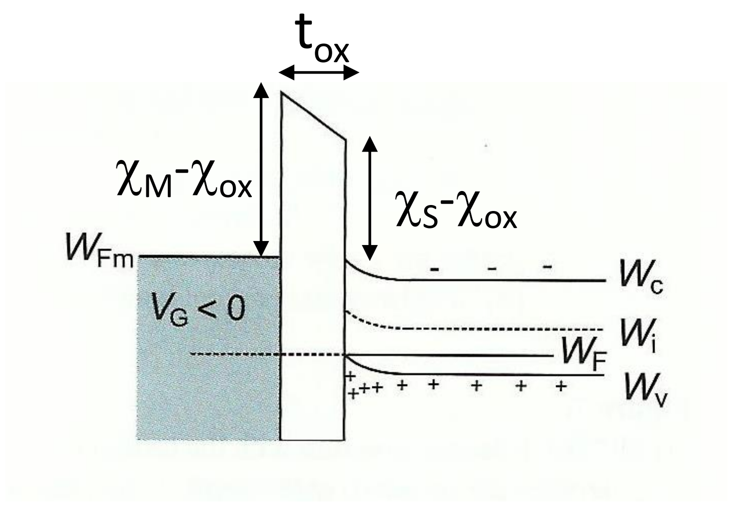
MŰEGYETEM 1782

April 1st, 2020

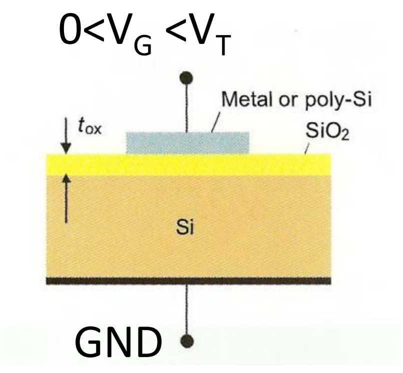
MOS capacitor operation (revision)

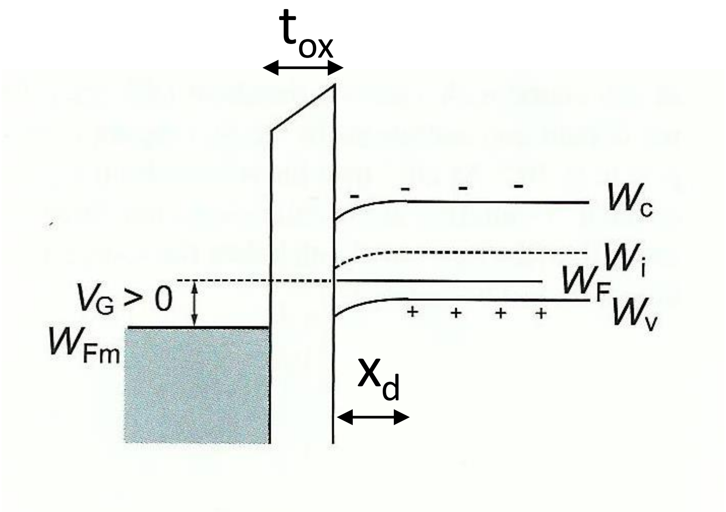
Accumulation



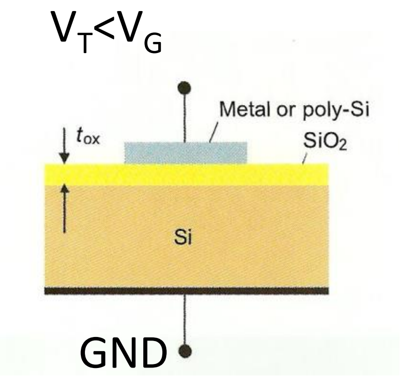


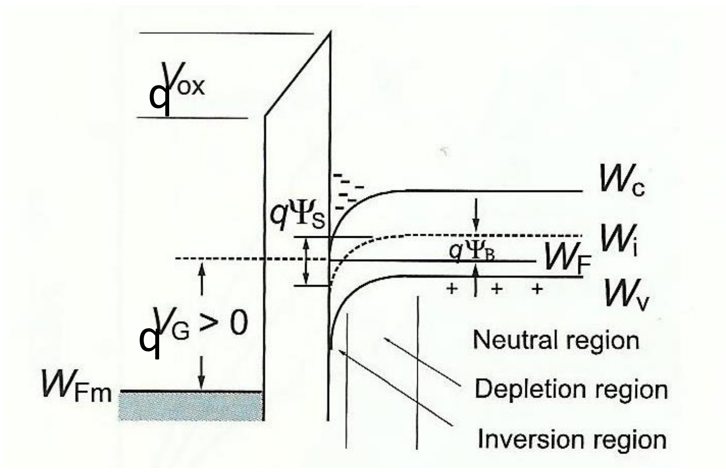
Depletion



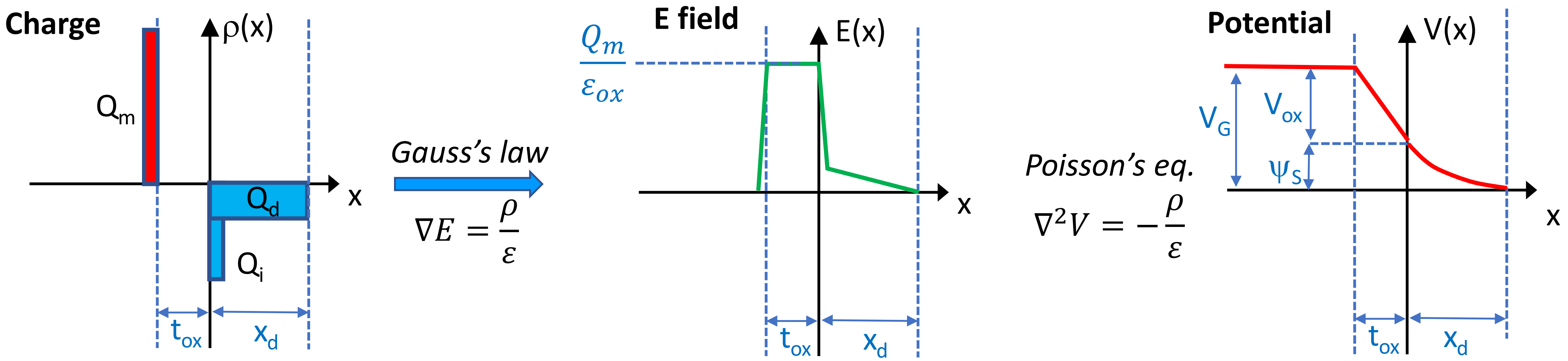


Inversion





MOS capacitor in inversion (revision)



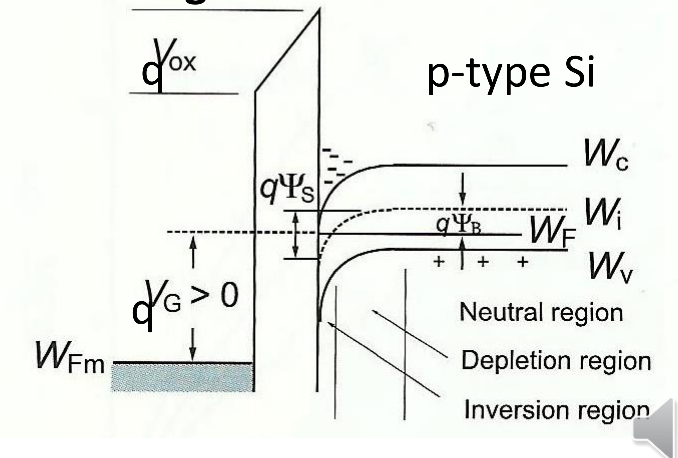
$V_G = \psi_s + V_{ox} = \psi_s + \gamma\sqrt{\psi_s}$ where $\gamma = \frac{\sqrt{2q\varepsilon_s N_A}}{C_{ox}}$

At strong inversion (def.): $\psi_s = 2\psi_B$ where $\psi_B \approx \frac{kT}{q} ln\left(\frac{N_A}{n_i}\right)$

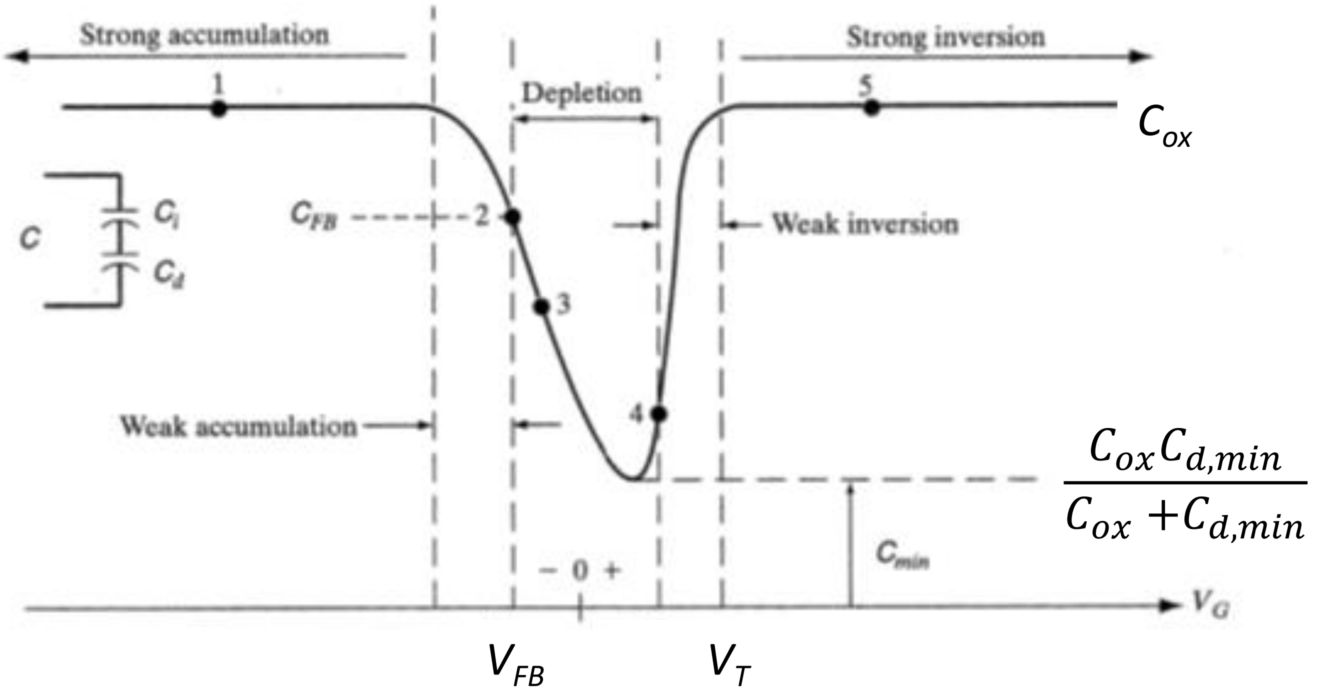
Threshold voltage (ideal): $V'_{T0} = 2\psi_B + \gamma\sqrt{2\psi_B}$

Threshold voltage (real): $V_{T0} = \underbrace{+\phi_{MS} - \frac{Q_{ss}}{C_{ox}} - \frac{Q_i}{C_{ox}}}_{V_{FB}} + 2\psi_B + \gamma\sqrt{2\psi_B}$

Band diagram



MOS capacitor in inversion (revision)



In strong inversion we can ignore weak inversion and depletion charges ($Q_i \gg Q_d$)→ $Q_i = C_{ox}(V_G - V_{T0})$

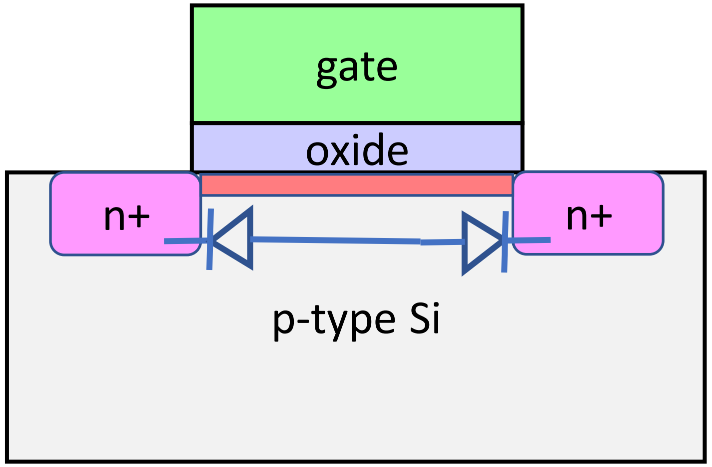
Overdriving voltage (V_{OV})

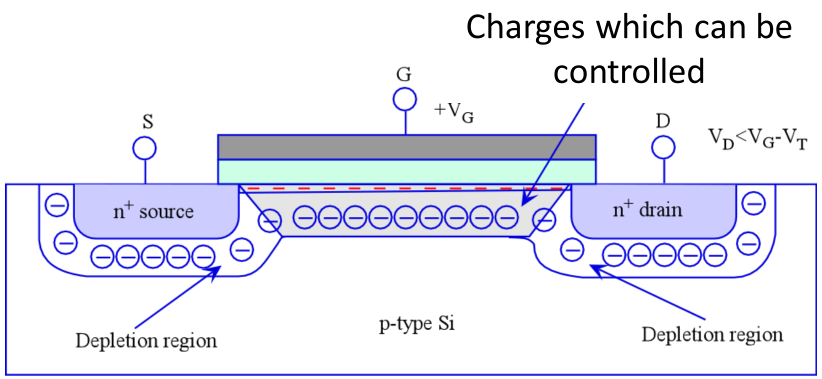
→ we can **control the interface charge** by the applied gate voltage → we can **make a device** out of it!

If $V_G < V_{T0}$ sub-trashold region (will be discussed later)

Let’s construct an (n-channel) MOS FET!

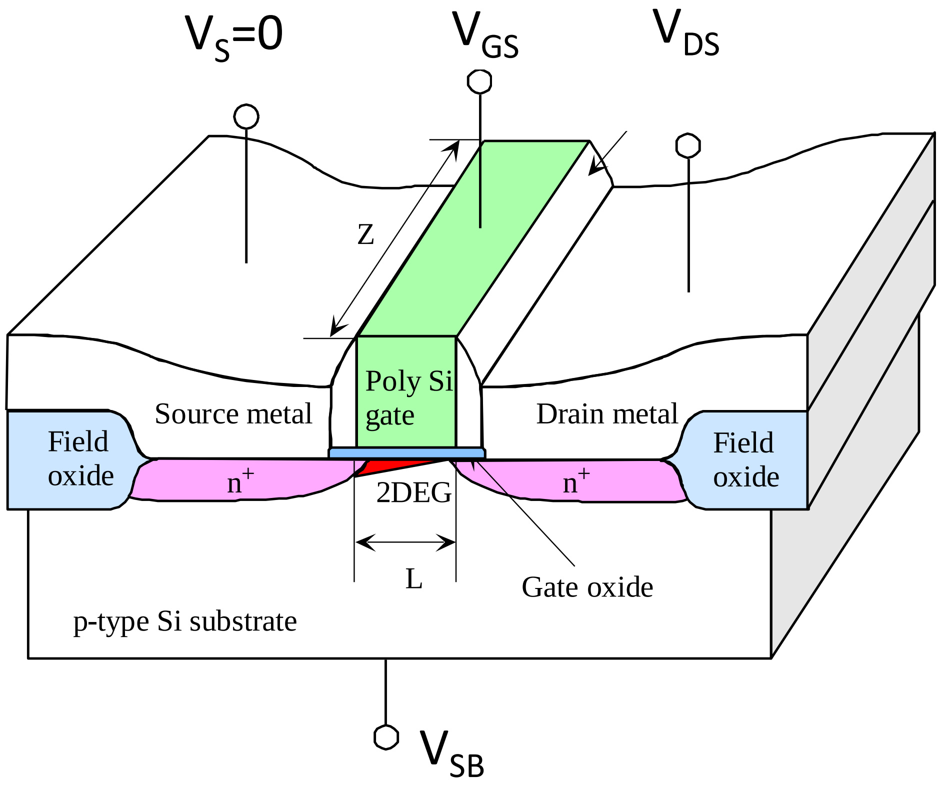
- We take a p-type Si substrate
- Gate/oxide stack to control the interface charge where gate is either metal or polycrystalline Si
- We need Ohmic contacts by forming highly n-doped pockets (ion-implantation)
- We don’t need to wait for the thermally generated minority charges → fast operation
- At low V_G no channel but a back-to-back p-n diode → it’s good since we can turn off the device
- By applying $V_G > V_{T,0}$ electron-channel (n) is formed at the interface on the semiconductor side





MOSFET is the most frequently manufactured device in history; ~13 sextillion (1.3×10^{22}) between 1960-2018.

„Classic” n-channel MOS FET



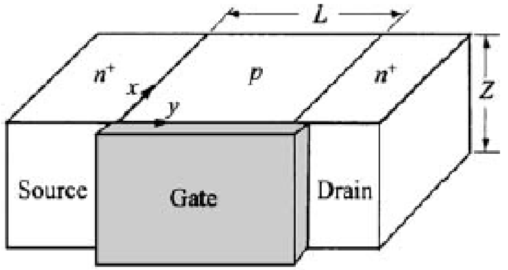
- **Source** terminal supplies charge carriers (reference electrode)
- **Drain** terminal sinks charge carriers
- **Gate** terminal controls the conduction between source and drain
- **Bulk** terminal on the substrate
- **L:** gate length
- **Z:** gate width (sometimes denoted by W)

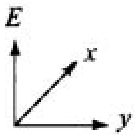
Bulk voltage affects the voltage drop on the oxide, therefore the threshold voltage (body effect):

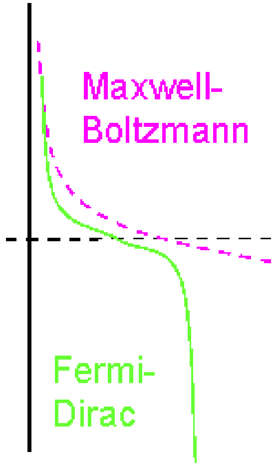
$$V_{T0} = V_{FB} + 2\psi_B + \gamma\sqrt{2\psi_B} \rightarrow V_T = V_{FB} + 2\psi_B + \gamma\sqrt{2\psi_B + V_{SB}}$$

Long channel MOS FET: 2D band diagram

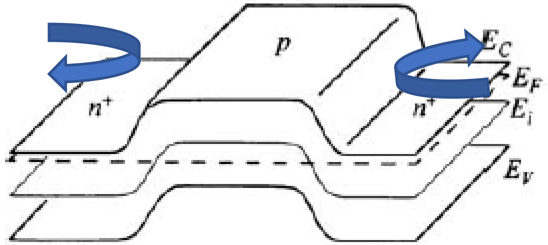
- Until now we have taken band diagram along x; Let’s extend it to x-y plane:





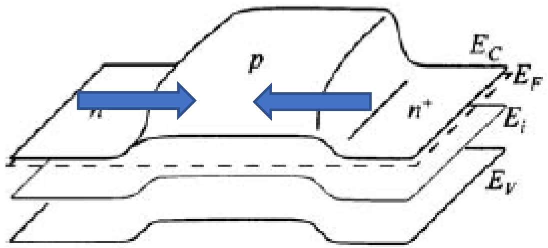


$V_{GS}=V_{FB}$, V_{DS}=0V



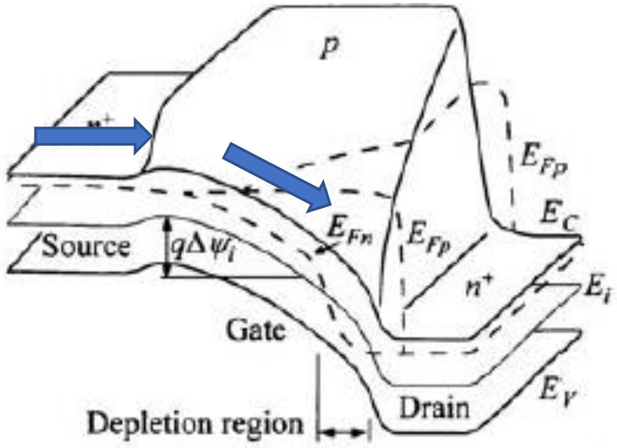
Electrons bounce back at the potential barrrier on both source and drain sides

$V_G>V_{FB}$, V_{DS}=0V



Some portion of the free electrons can fill up the n-channel from both source and drain sides (I_{DS}=0)

$V_G>V_{FB}$, V_{DS}>0V

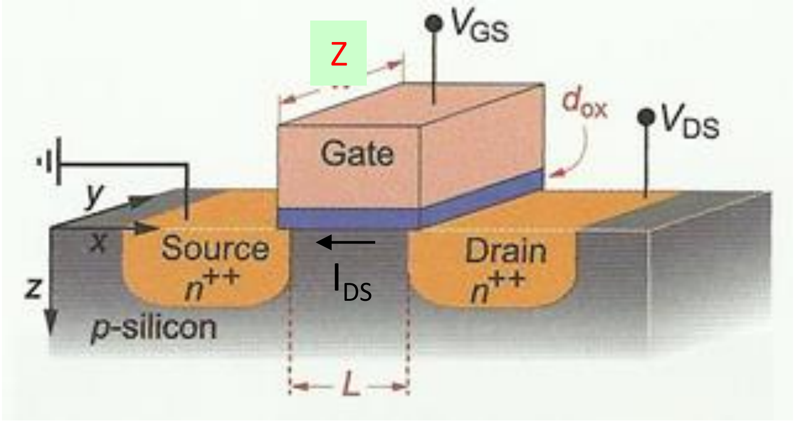


Electrons are driven by the field toward drain (I_{DS}>0).

Drain-source current : uniform charge sheet model

Let's assume $V_{GS} > V_T, V_{DS} \ll V_{GS} - V_T\ (small) \rightarrow Q(y) = Q_i\ (fixed\ in\ the\ channel)$ $\qquad Q_i(y) \approx Q_i$

In inversion region: $Q_i = C_{ox}(V_{GS} - V_T)$



Overall amount of charges below the gate:

$$q_{inv} = Z \cdot L \cdot C_{ox}(V_{GS} - V_T)$$

Drain source current: $I_{DS} = \dfrac{q_{inv}}{\tau_F}$

τ_F: transfer time needed to replace a slab of charge with a new one → $\tau_F = \dfrac{L}{v_D}$

v_D: drift velocity, the average velocity of the electrons induced by the electric field

At relatively low electric field (E<2·10³ V/cm for Si) μ is constant: $v_D = \mu \cdot E = \mu \dfrac{V_{DS}}{L}$ $\quad \rightarrow \tau_F = \dfrac{L^2}{\mu V_{DS}}$

$$I_{DS} = \mu C_{ox} \frac{Z}{L}(V_{GS} - V_T) V_{DS}$$

G

$I_{DS} \propto V_{DS}$, where the conductance is modulated by V_G

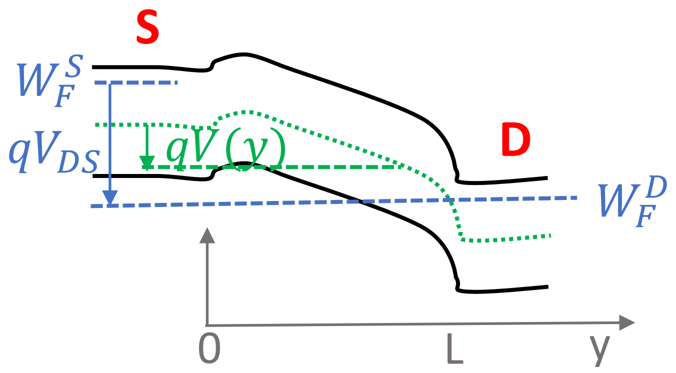
(The operation principle was invited by Julius Lillienfeld in 1928!)

Drain-source current: non-uniform charge sheet model

Let's assume $V_{GS} > V_T$, $V_{DS} < V_{GS} - V_T$ and $V_T(y) = V_T$

$$Q_i(y) = C_{ox}\big(V_{GS} - V_T - V(y)\big) \qquad V(y) = \frac{W_i(x=0,y=0) - W_i(x=0,y=0)}{q}$$

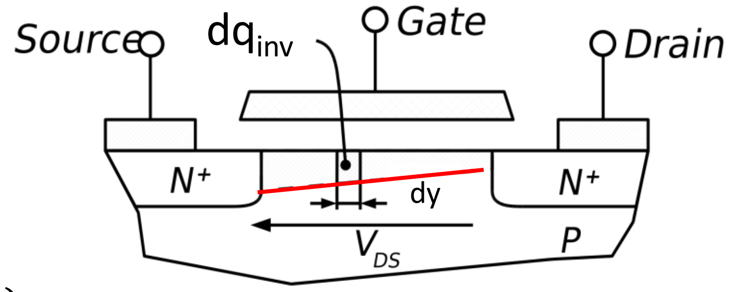
→ $Q_i(y)$ is decreasing from source to drain



Charge of an infinitesimal section: $dq_{inv} = Z \cdot dy \cdot C_{ox}\big(V_G - V_T - V(y)\big)$

Drain-source current is fixed along the channel: $I_{DS} = \dfrac{dq_{inv}}{d\tau_F} = \dfrac{v_D\, dq_{inv}}{dy}$

→ $v_d(y)$ and $dq_{inv}(y)$ change in unison to keep the current constant



Let's assume again that μ is constant in this field region → $v_D = \mu E = \mu \dfrac{dV}{dy}$

$$I_{DS} = \mu \frac{dV}{dy^2} Z \cdot dy \cdot C_{ox}\big(V_G - V_T - V(y)\big) \qquad \int_0^L dy\, I_{DS} = \mu C_{ox} Z \int_0^{V_{DS}} \big(V_G - V_T - V(y)\big)dV$$

$$I_{DS} = \mu C_{ox} \frac{Z}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}{}^2}{2}\right]$$

Triode region (also referred as linear or Ohmic region)

If we take into the account the change of the threshold voltage ($V_T(y) \neq V_T$) along the channel the integration is more complicated

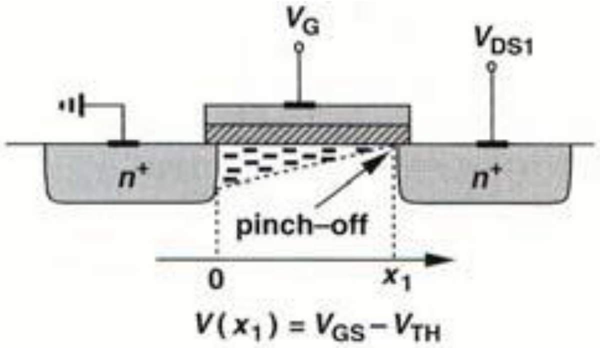
→Bulk charge theory

MOS FET pinch-off region

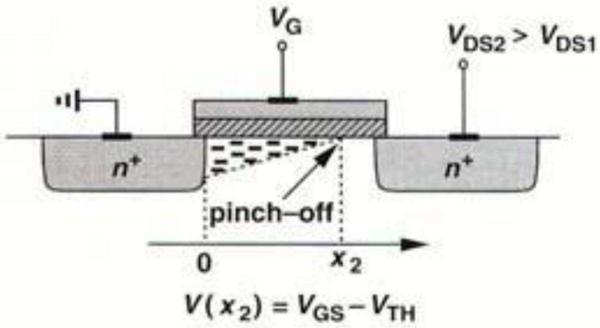
What happens if $V_{GS} > V_T, V_{DS} = V_{GS} - V_T$?

$$Q_i(L) = C_{ox}(V_{GS} - V_T - V_{DS})=0$$

→ strong inversion stops at the edge of the drain: onset of **pinch-off**



If $V_{DS} > V_{GS} - V_T$ → pinch-off position shifts toward the source



$$L \rightarrow L_{eff}, \text{ where } V_{GS} - V_T = V(L_{eff})$$

Potential drop between L and L_{eff} : $\Delta V = V_{DS} - V_{GS} - V_T$

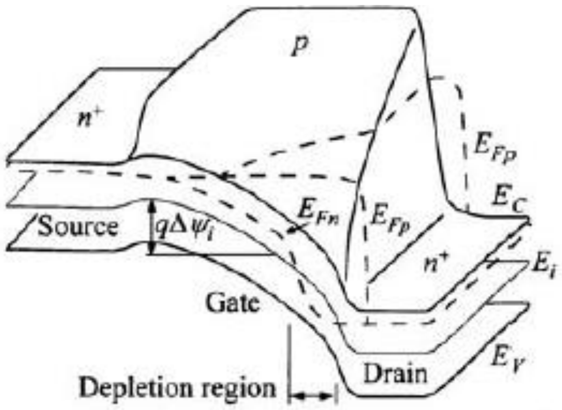
I_{DS} is not stopped but not really controlled by V_{DS}

$$I_{DS} = \mu C_{ox} \frac{Z}{L} \left[(V_G - V_T) V_{DS} - \frac{{V_{DS}}^2}{2} \right]$$

↓

$$I_{DS} = \frac{\mu C_{ox} Z}{2 L_{eff}} (V_{GS} - V_T)^2 \approx \frac{\mu C_{ox} Z}{2L} (V_{GS} - V_T)^2$$

Saturation region



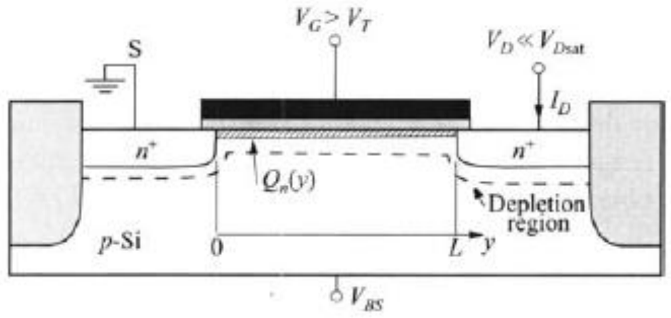
Long channel MOS FET

$V_{GS} > V_T$

Triode region

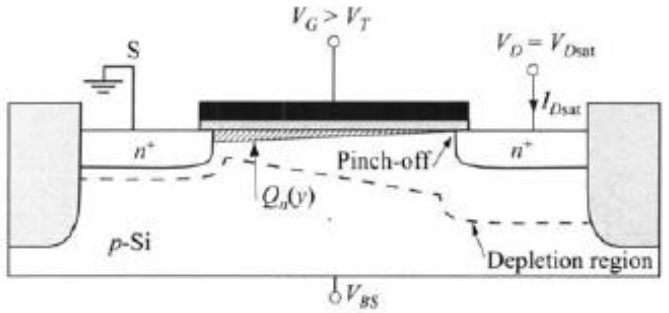
$V_{DS} < (V_{GS} - V_T)$

$$I_{DS} = \mu C_{ox} \frac{Z}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$



Onset of pinch-off

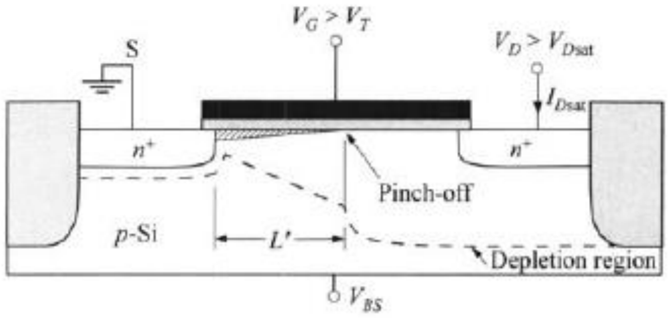
$V_{DS} = (V_{GS} - V_T)$

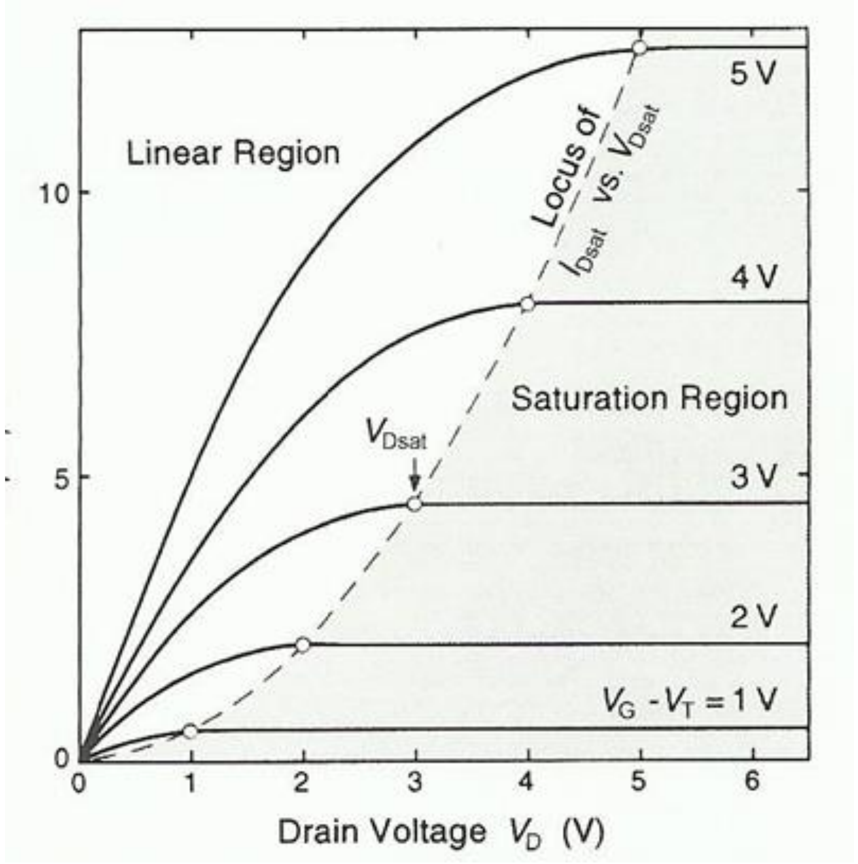


Saturation

$V_{DS} > (V_{GS} - V_T)$

$$I_{DS} = \frac{\mu C_{ox} Z}{2L} (V_{GS} - V_T)^2$$





Electron mobility and transconductance

- The free carrier mobility in the inversion channel can be significantly different from the bulk value $\mu_{eff} < \mu_{bulk}$ mainly because of the interface scattering. → I_{DS} expressions have to be refined.

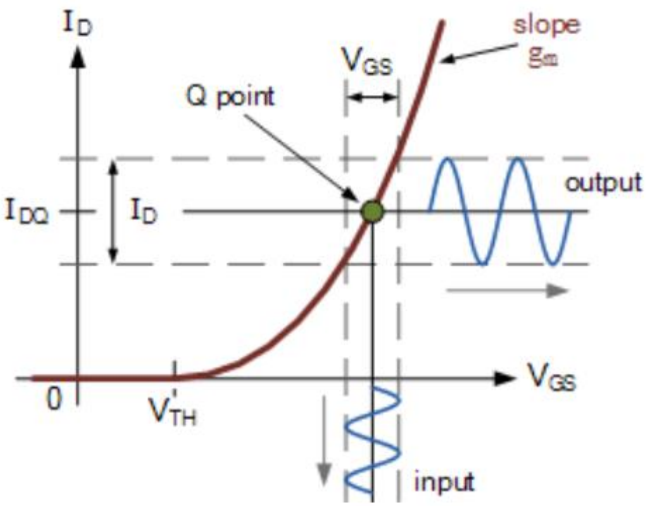
- μ_{eff} can be experimentally determined from the transconductance curve. It is common way to characterize the quality of the channel layer or nanowire.

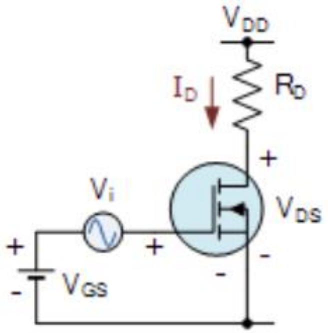
$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS,constant}}$$

→ for triode region: $g_m = 2\mu_{eff}\frac{Z}{L}C_{ox}V_{DS}$

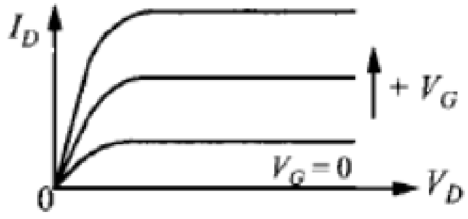
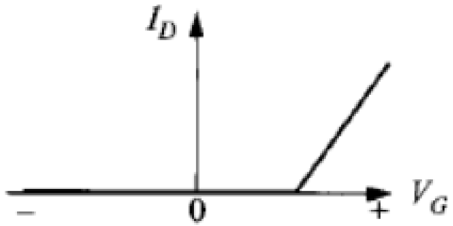
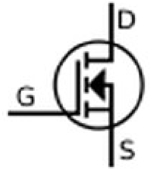
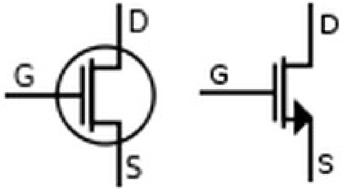
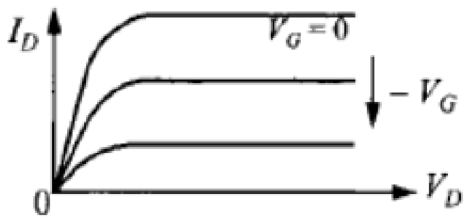
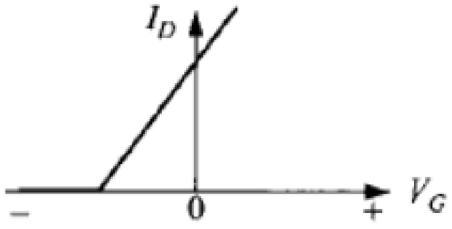
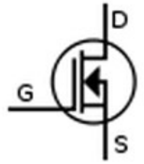
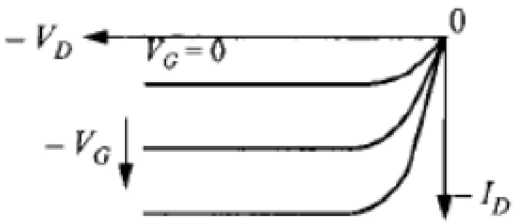
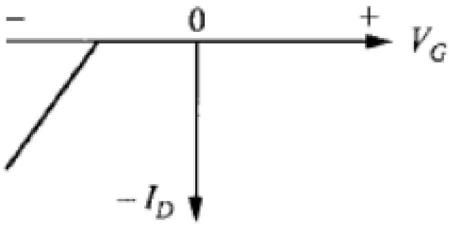
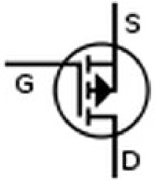
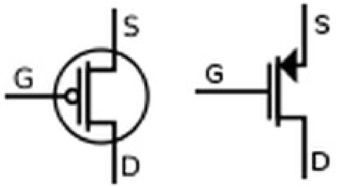
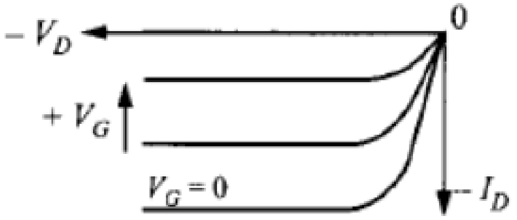
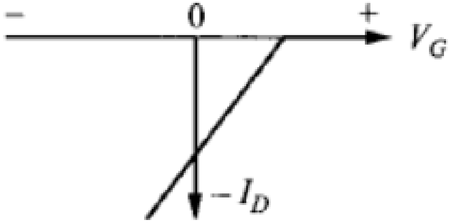
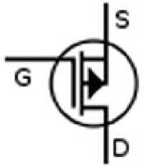
→ for saturation region: $g_m = 2\mu_{eff}\frac{Z}{L}C_{ox}(V_{GS} - V_T)$

- transconductance is also often used to analyze the gain of the transistor as an amplifier





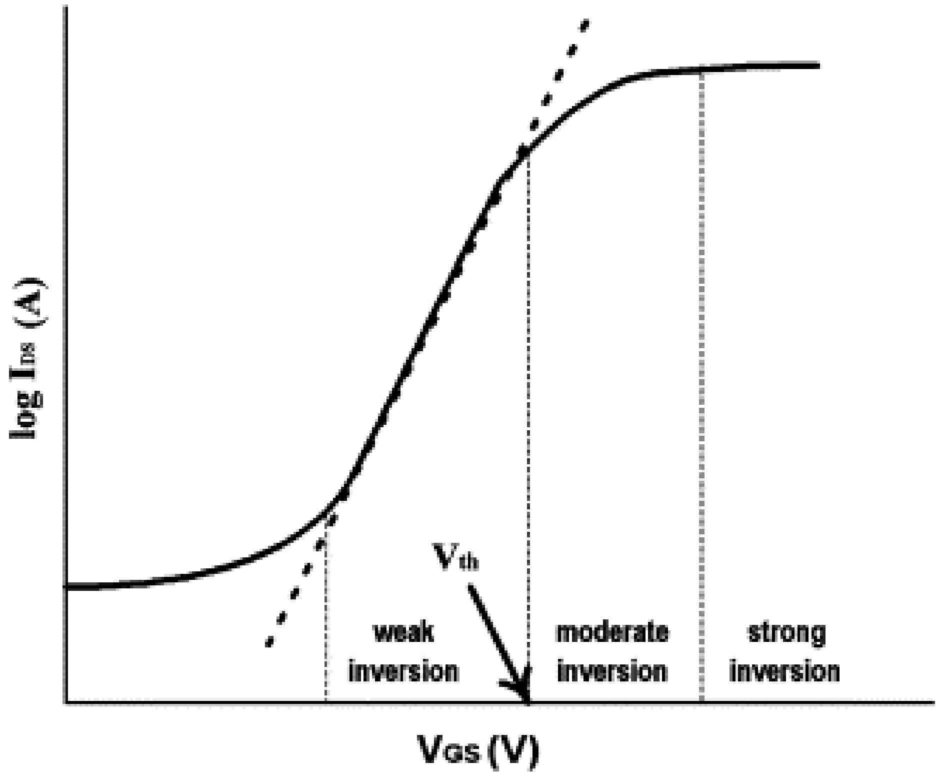
Types of MOSFET

	Mode	I_D vs. V_D	I_D vs V_G	With bulk	Without bulk
N-channel	Enhancement (Normally-off)				
	Depletion (Normally-on)				
P-channel	Enhancement (Normally-off)				
	Depletion (Normally-on)				

OFF-state: sub-threshold region

What happens if $V_{GS} < V_T$?

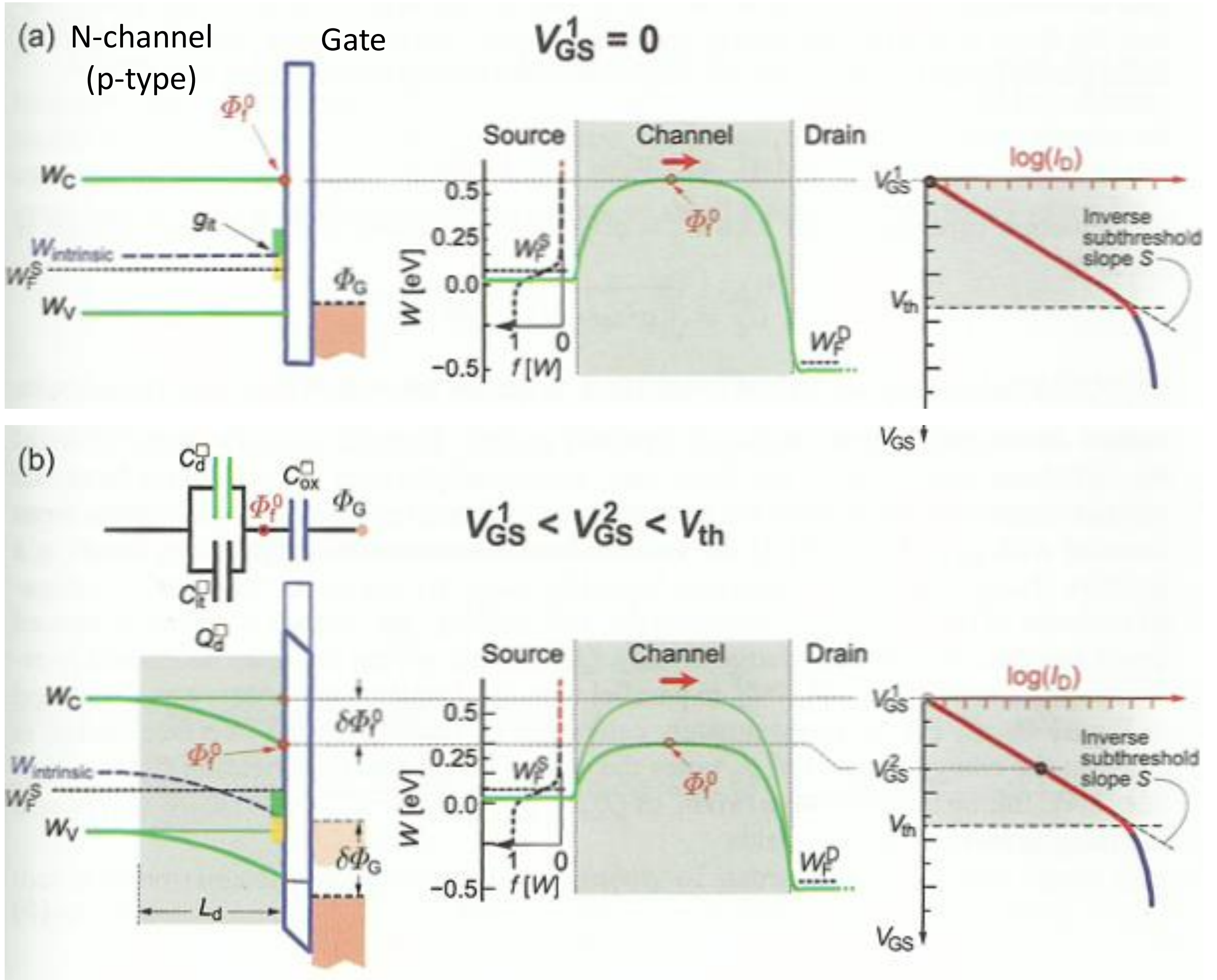
- $Q_i = C_{ox}(V_{GS} - V_T)$ equation is not valid anymore because we are in the weak inversion or depletion region
- We still have current, but low



OFF-state: sub-threshold region

N-channel in p-type below the gate

x: normal to the channel — y: parallel to the channel — transconductance



- In sub-threshold region diffusion current dominates over the drift current
- Subthreshold swing:

$$S = \left[\frac{\partial log(I_{DS})}{\partial V_{GS}}\right]^{-1} = \frac{k_B T}{q} ln(10) \left[1 + \frac{C_d + C_{it}}{C_{ox}}\right]$$

$$\text{if } C_{ox} \gg C_d + C_{it} \rightarrow S = \frac{k_B T}{q} ln(10) \approx 60 \frac{mV}{dec}$$

- This is **the smallest possible S of any transistor** whose switching relies on the modulation of carriers injected from a thermally broadened Fermi function
- This is the **major obstacle** to further reducing the operational voltage and hence power consumption