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NANOSENSORS
Centre for Energy Research
Institute of Technical Physics and Materials Science

ADVANCED SEMICONDUCTOR DEVICES

02_CMOS_Technology

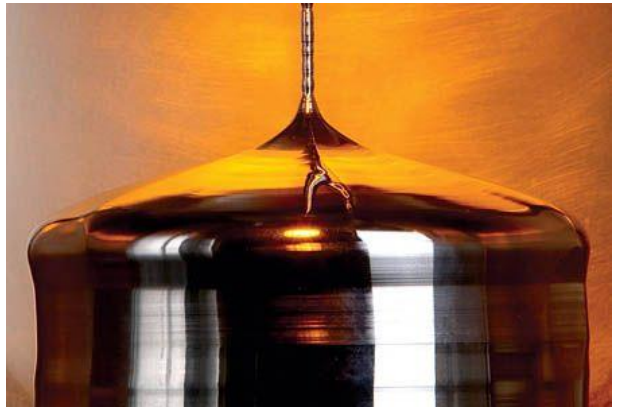
February 12nd, 19th, 2020

Stages of semiconductor manufacturing

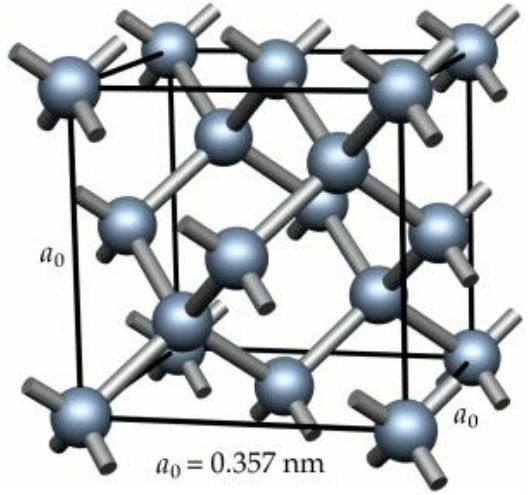
- **Material preparation:** Sand to polycrystalline silicon
- **Crystal growth and wafer preparation:** Polycrystalline silicon to wafer
- **Wafer fabrication** Circuit/devices formed in/on wafer surface
- **Packaging** Functioning die placed in a protective package

Si single crystal

High quality single crystal in large size



Single crystal Si grown by Czochralski method



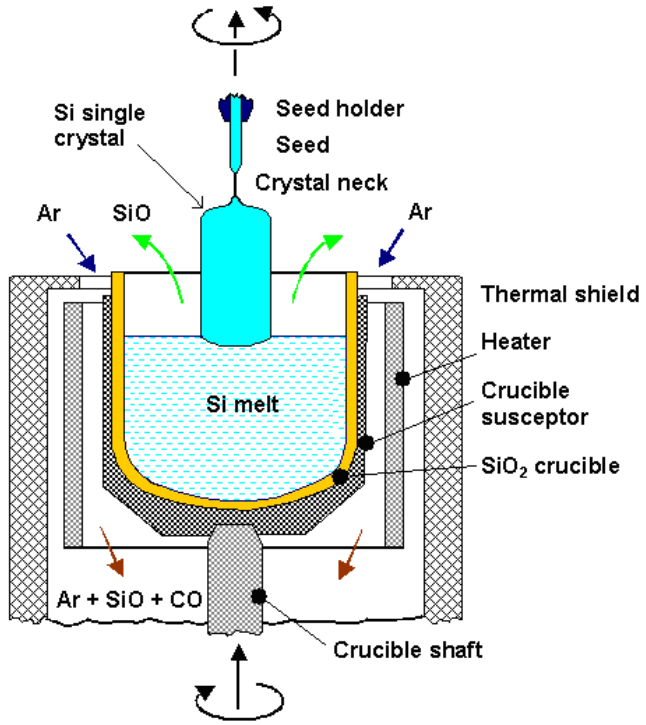
Face centered cubic crystal (fcc)

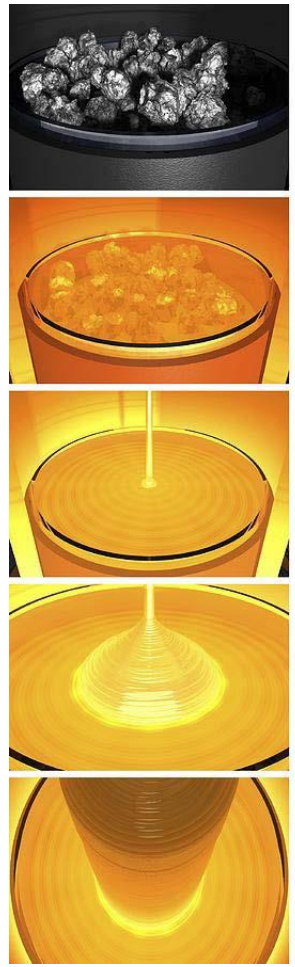
+ advantageous physical properties and good quality native oxide

- Microelectronics is based on mainly on **Si**.
- III-V semiconductors play an important role in optoelectronics.

Czochralski method

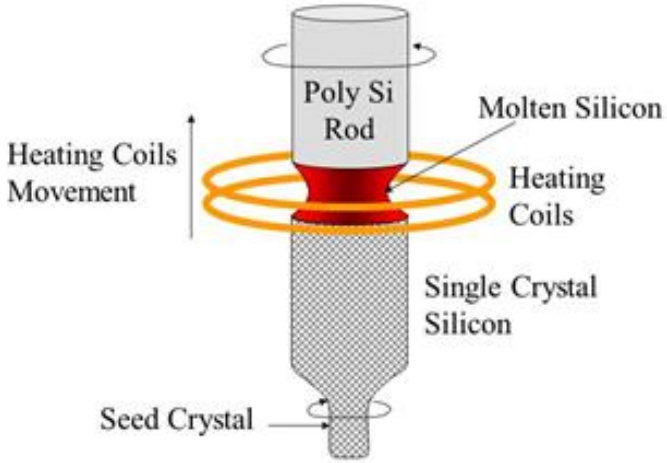
- Polysilicon nuggets with the dopants are melted in the quartz crucible at a T>1400°C
- Purity of the polysilicon nuggets 99.9999999% (9N)
- Si crystal Si crystal with the desired orientation (<100>, <110> , <111> is slowly pulled out; both the seed and the crucible is rotated to maintain homogeneity
- Typical impurity concentration: N_O: 10^{18} cm^{-3}, N_C: 10^{16} cm^{-3} (N_{Si}=$5 \cdot 10^{22}$ $1/cm^3$)





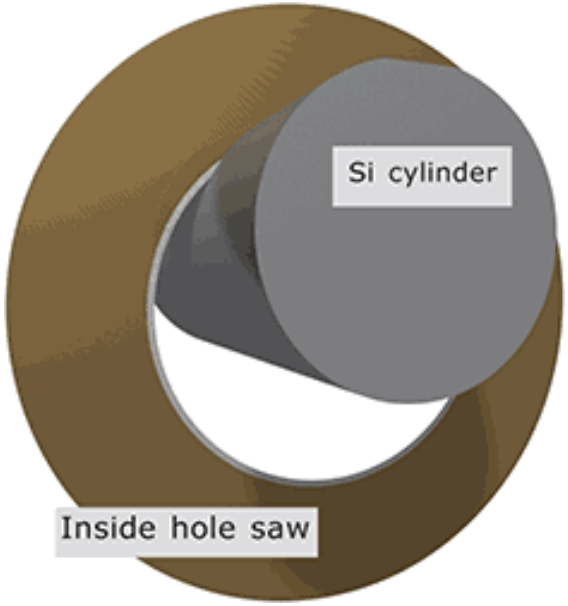
Floating zone method

- No vessel is needed → higher purity than for CZ
- Carrier concentration down to 10^{11} cm^{-3} → highly resistive wafers (1-10 kOhm·cm)
- Max diameter is 150 mm because of the surface tension limitation
- Evacuated chamber or filled with inert gas
- Molten zone carries the impurities away from the c-Si → reduces impurity concentration (most impurities are more soluble in the melt than the crystal)
- Higher price compared to CZ
- Doping by dopant gases, such as PH_3, AsH_3, B_2H_6
- Mainly used for power devices



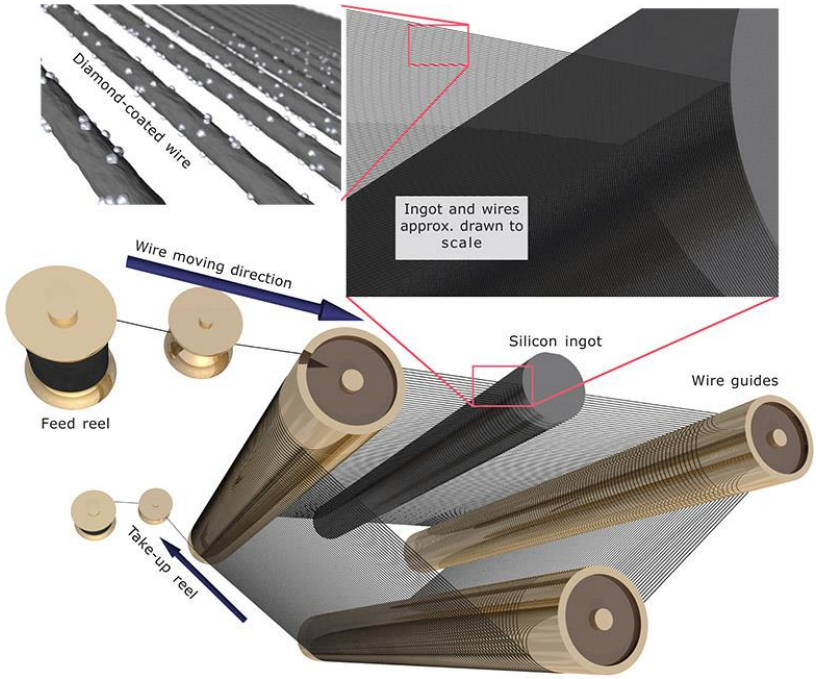
Wafer processing

Annular saw



- Wafer surface is relatively smooth, subsequent steps takes less time
- Low throughput

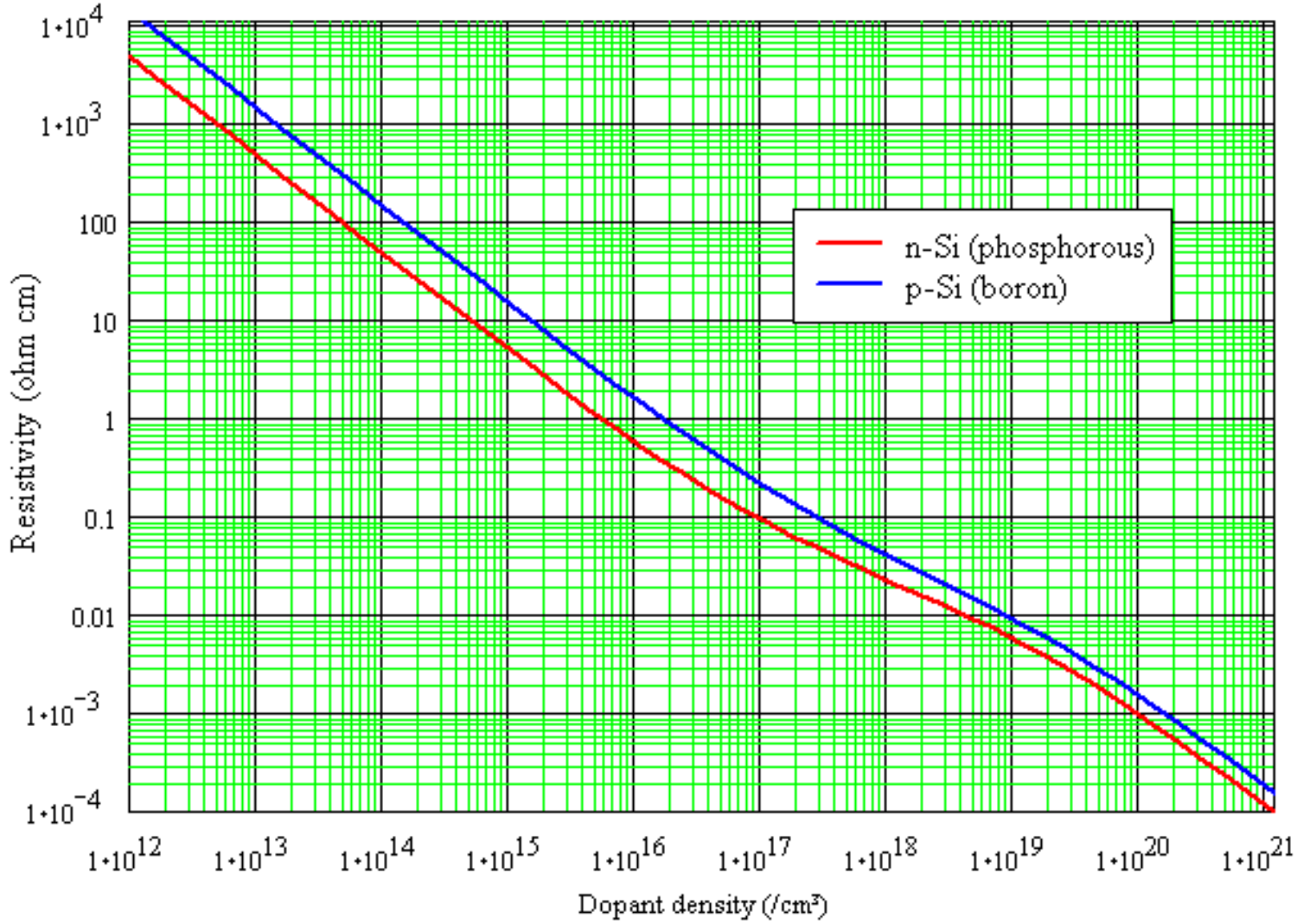
Wire saw



- Wafer surface is less smooth, subsequent lapping takes more time
- High throughput

The process is continued and finished by lapping, etching, polishing and cleaning

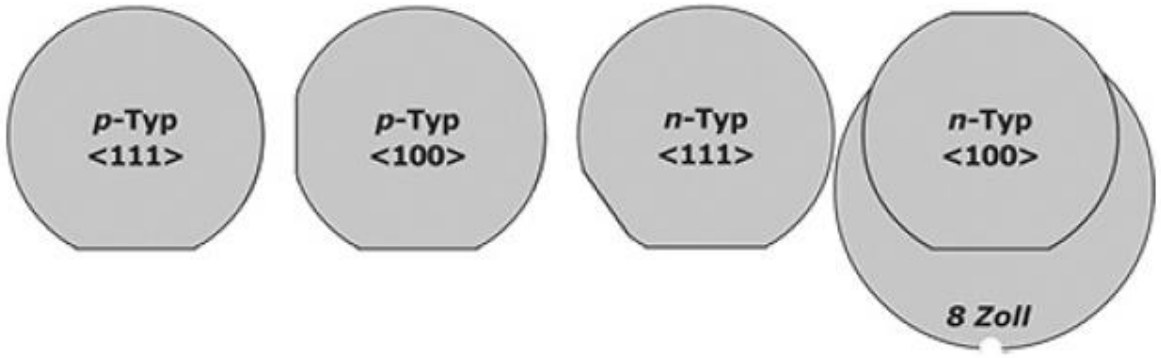
Wafer doping



Si wafer specification

Diameter (mm)	Growth	Dopant	Orientation	Finish	Coating
☐ 50.8	☐ CZ	☐ B	☐ <100>	☐ Single Side	☐ With
☐ 76.2	☐ FZ	☐ Ph	☐ <111>	☐ Double Side	☐ Without
☐ 100		☐ Sb	☐ <110>	☐ As Cut	
☐ 125		☐ As		☐ As Lapped	
☐ 150		☐ Undoped		☐ Ground	
☐ 200		☐ Intrinsic		☐ Etched	
☐ 300					

TTV	Bow	Warp	Thickness	Resistivity
≤ ☐	≤ ☐	≤ ☐	min ≥ ☐	min ≥ ☐
			max ≤ ☐	max ≤ ☐




12” Si wafer (300 mm)

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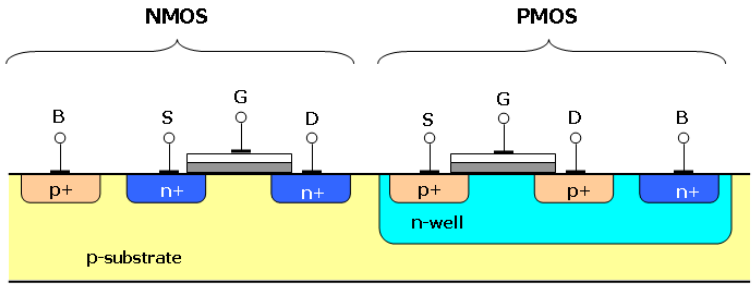
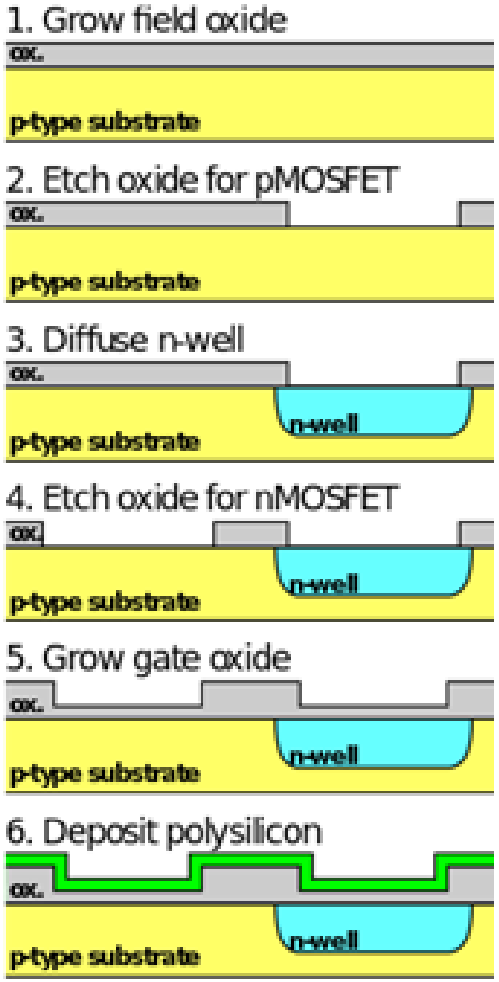
Wafer/chip processing techniques

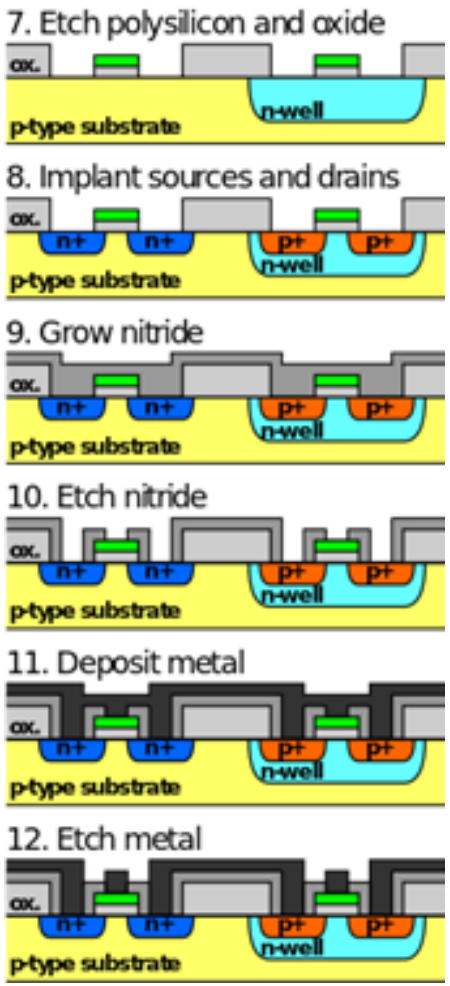
I) Modifying methods	II) Additive methods	III) Subtractive methods
Ion Beam Treatment • Implantation • Amorphization • Smart-cut	**Thin film deposition** • Chemical Vapor Deposition (CVD) • Physical Vapor Deposition (PVD) • Chemical solution deposition (CSD) • (Thermal growth)	**Etching** • Wet chemical etching • Ion beam etching • Reactive Ion Etching
Radiative treatment • Resist exposure • Polymer hardening	**Printing techniques** • Ink-jet printing • Microcontact printing	**Tool-Assisted Material Removal** • Chemical-mechanical polishing (CMP) • Chipping • Drilling
Thermal annealing • Crystallization • Diffusion • Change of phase • (Thermal growth)	**Assembly** • Wafer bonding • Surface mount technology • Wiring and bonding methods	

CMOS fabrication process



- Si wafer manufacturing
- Thermal oxidation
- Doping by ion implantation
- Physical vapor deposition
- Chemical deposition
- Lithography
- Etching
- Back-end process



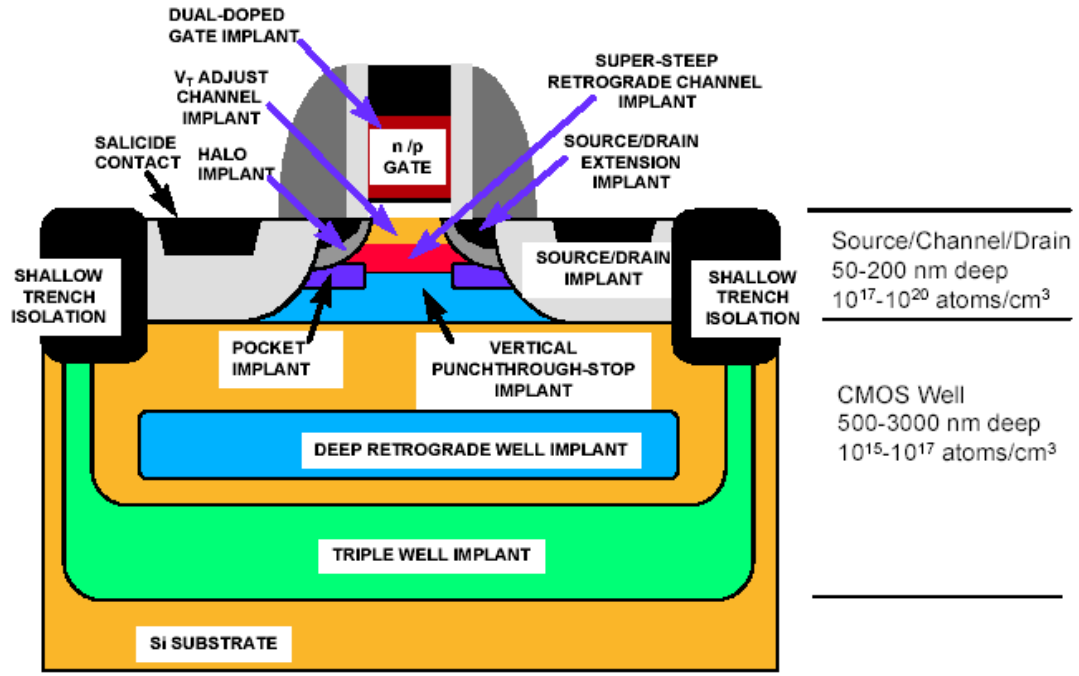


Ion implantation

Doping by ion implantation

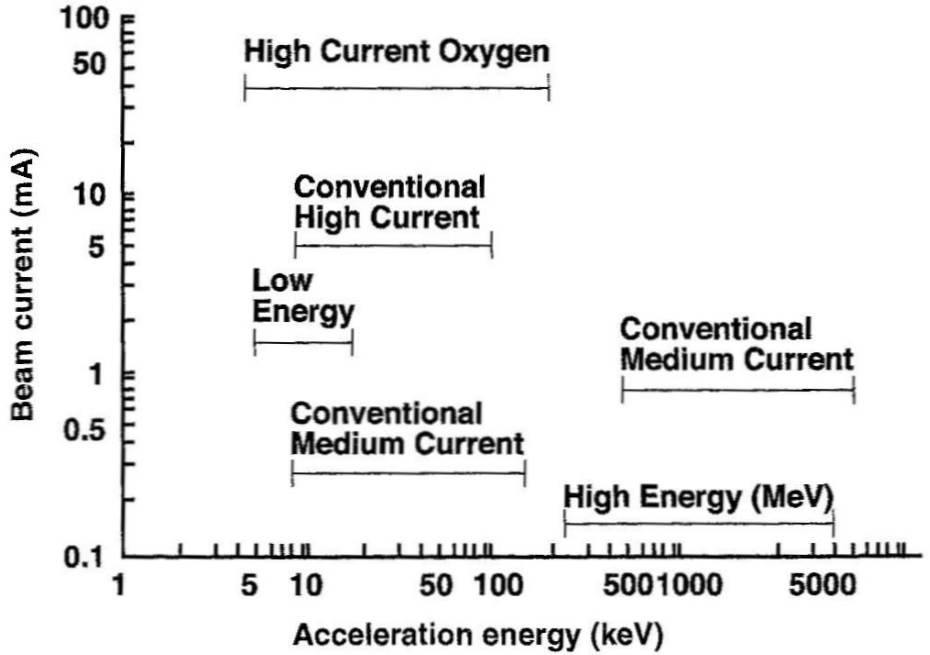
- Several advantages comapred to diffusion
- Ions are accelerated into a solid target for doping (e.g. for step 3)
- Both kinetic energy and dose can be accurately controlled
- Ultra thin junctions can be made
- Excellent doping uniformity across the wafer (< 1% variation across 12” wafer) and from wafer to wafer.
- Can be masked by thin films like photoresist or oxide
- Dopants are thermally activated after ion-implantation (substitutional position)
- Typical parameters:
  - Type of ion: P, As, Sb, B, O etc.
  - Dose (D, # of atoms/cm^2): 10^{11}-10^{18} cm^{-2}
  - Concentration (C, # of atoms/cm^3), $\mathrm{D} = \int_0^\infty C(x)dx$
  - Ion flux (Φ=D/t) 10^{12}-10^{14} cm^{-2}s^{-1} , i.e. ~100nA-10 μA
  - Acceleration energy: ~100ev- 1 MeV

Doping by ion implantation

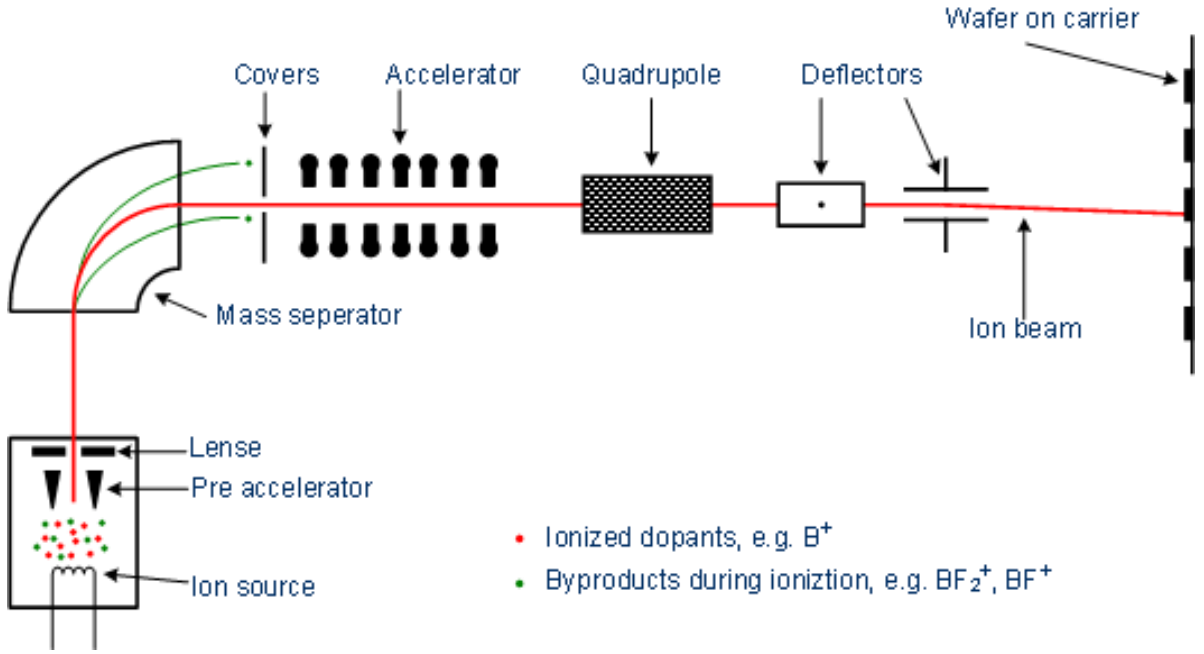


9-10 different ion implantations during the full process!

Ion implanters

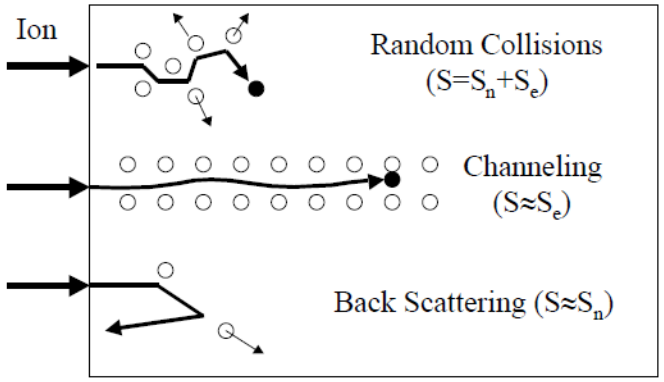


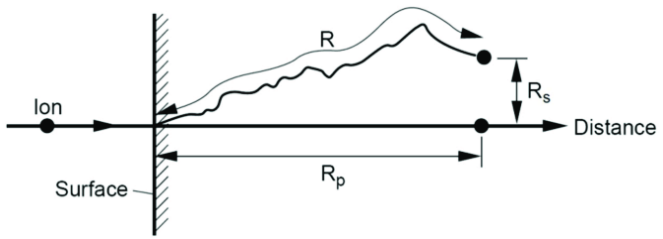
Ion implanter

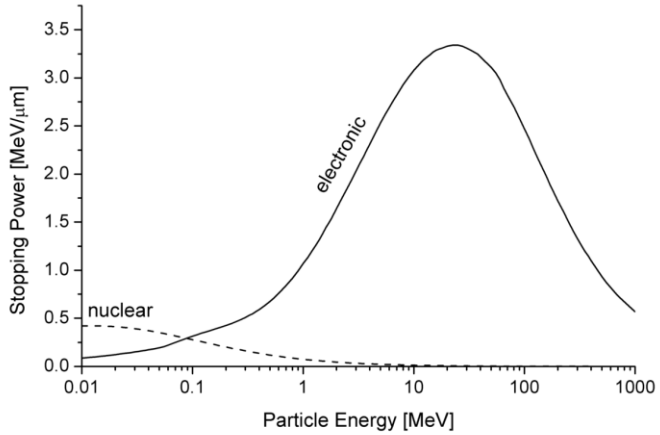


- **Ion source:** ionization chamber operating at high voltage (25-60 kV) and converts the electrically neutral dopant atoms into plasma ions in the gas phase (Arsine, Phosphine, Diborane, BF_3) (p~1 mTorr). Ionizing electrons are emitted from the filament.
- **Mass separator:** a magnet bends the ion beam through right angle and selects the desired impurity ion and purge undesired species. Selected ion passes through an aperture $\left(\frac{1}{2}mv^2 = V_{ext}q; qvB = M\frac{v^2}{R} \rightarrow \frac{M}{q} = \frac{R^2B^2}{2V_{ext}}\right)$
- **Accelerator:** adds energy to the beam up to 5MeV.
- **Scanning system:** x and y axis deflection plates to scan the beam across the wafer to produce uniform implantation of desired dose.

Doping by ion implantation







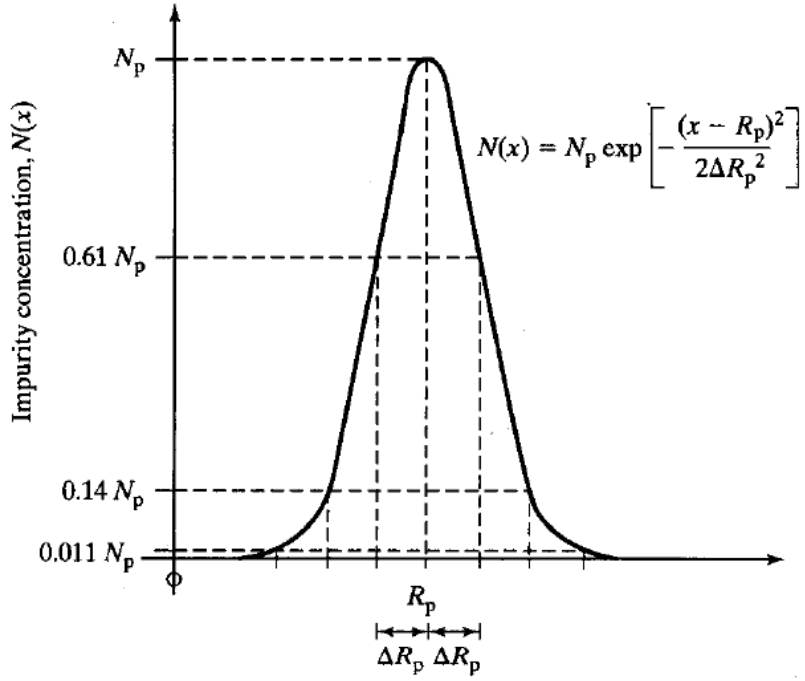
- Stopping power (S): retarding force acting on the charged particles due to interaction with matter, resulting in loss of particle energy

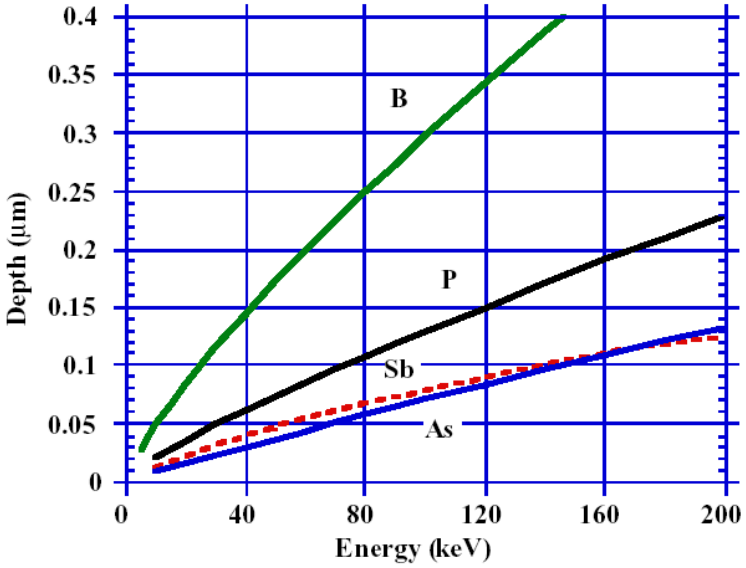
$$S(E) = -\frac{dE}{dx} \qquad \text{Projected range:} \qquad R_P = \int_0^{E_0} \frac{1}{S(E)}\, dE$$

- At the beginning at high energies the ion is slowed down mainly by the electron cloud (**electronic stopping**, S_e)
- When the ion has slowed down the collisions with nuclei become more and more probable (**nuclear stopping**, S_n)
- When atoms of the solid receive significant recoil energies when struck by the ion, they will be removed from their lattice positions, and produce a **cascade of** further **collisions** in the material. These collision cascades are the main cause of **damage** production during ion implantation in metals and semiconductors.

Doping by ion implantation

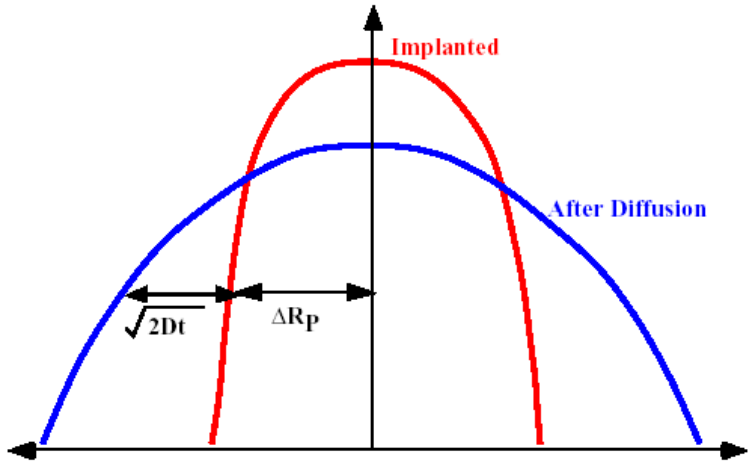
- Gaussian distribution for first order approximation.
- R_p: projected range (function of ion energy and mass, and atomic number of impurity as well as target material)
- ΔR_p: straggle (standard deviation)
- N_p = peak concentration at x=R_p.
- Dose: $\sqrt{2\pi}N_p\Delta R_p$

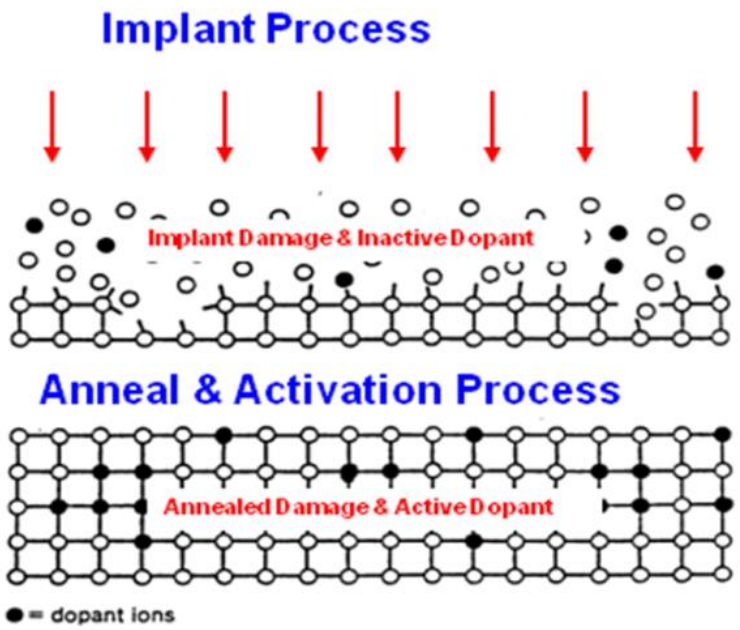


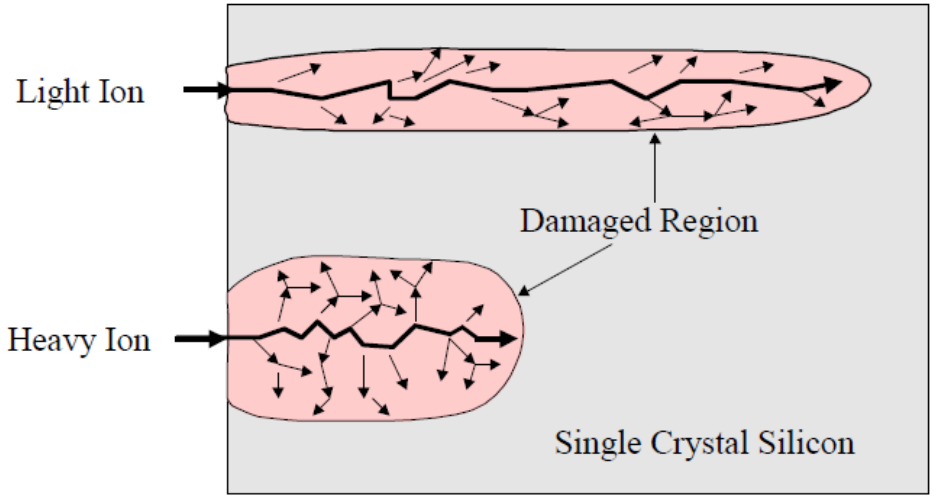


Ion implantation + annealing

- Dopant has to be activated, that is bonded with four Si atoms (interstitial position)
- Annealing helps to recover damaged crystals
- Accompanied with the broadening of the profile which can be wanted or unwanted

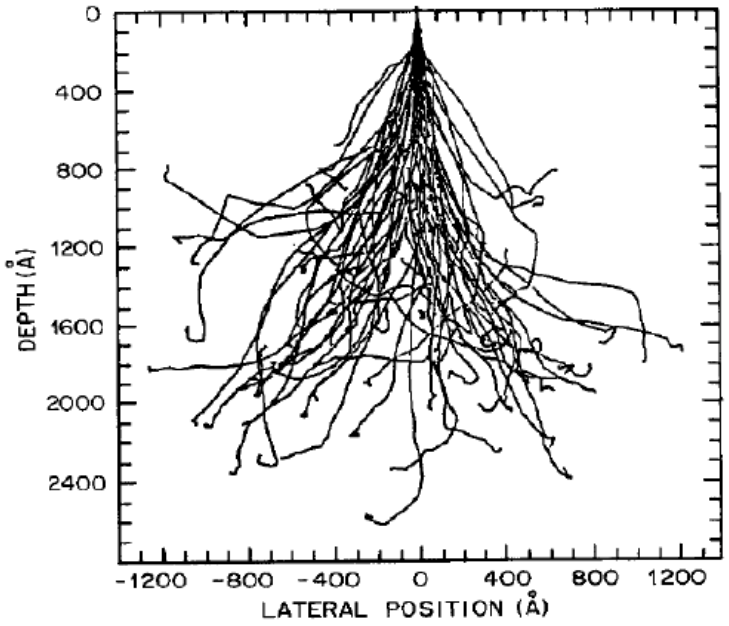


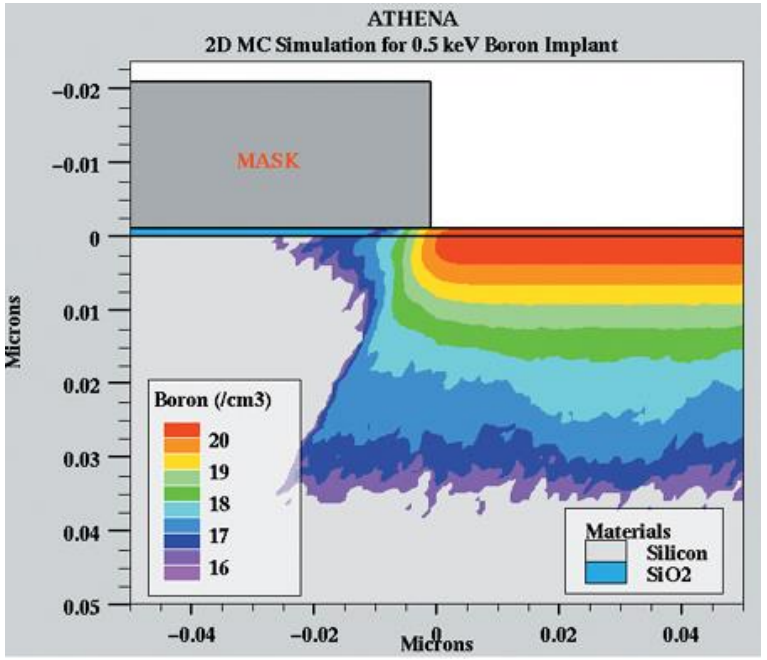




2D/3D simulation of implantation profiles

- E.g. Monte Carlo simulation techniques (SRIM&TRIM, Athena/Silvaco)
- Design of the mask layer thickness
- Calculation of the p/n junction's location
- Design multiple implantation
- Simulate the effect of annealing

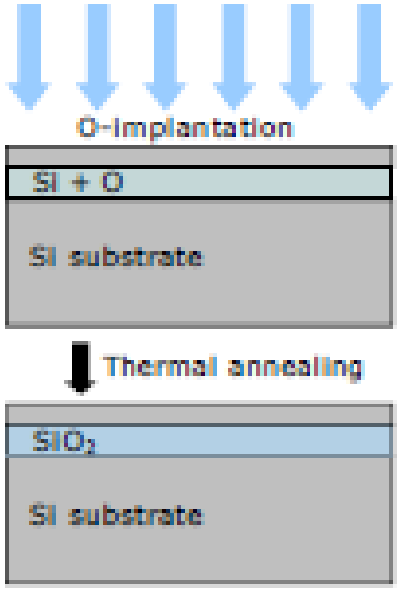




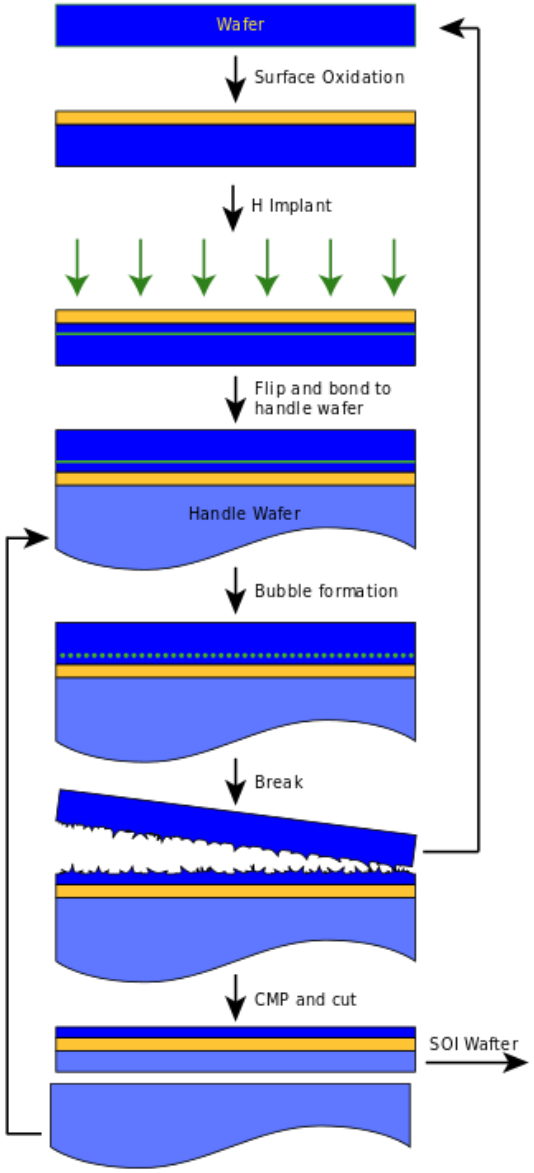
Silicon on Insulator (SOI) wafer by ion implantation

- Thin single crystal Si layer (device) on a buried oxide (BOX)
- To reduce parasitic device capacitance and leakage current
- Also often used for microelectromechanical systems (MEMS): membrane and cantilevers

Simox process



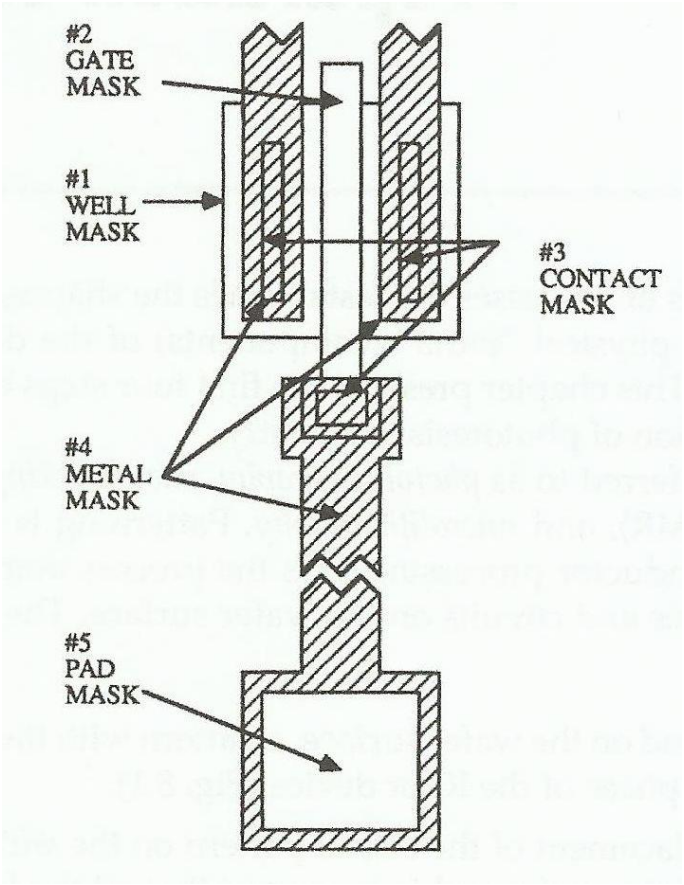
Smart cut



Patterning process

Patterning process

Pattering is one of the most critical operations in semiconductor processing. An **IC** wafer-fabrication process can require **40 or more** individual patterning steps



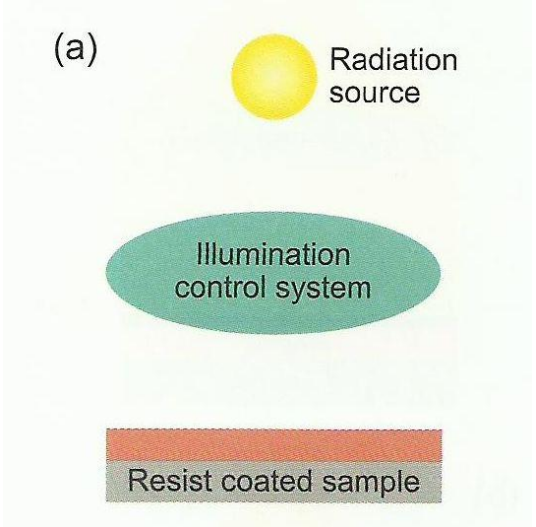
Goals of the operation

- To **create**, in and on the wafer surface, **a pattern with the dimensions** established **in the design** phase of the IC
- The **correct placement** of the circuit pattern on the wafer relative to the crystal orientation of the wafer and in a manner that all the layer **parts are aligned**

Photolithography

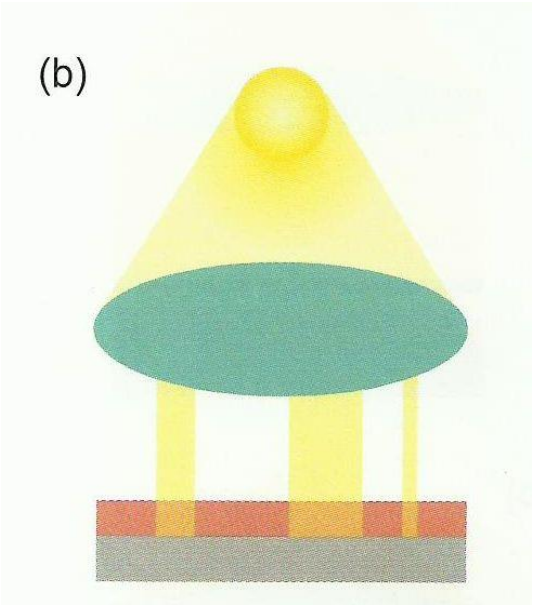
- In microelectronics the most typical method to define a pattern is called **lithography**
- **Lithography** is traditionally a color printing method (λιθοζ- lithos: stone + γραφειν - graphein: to write) where a partially hydrophilic piece of stone or metal plate was immersed into ink and transferred to a substrate

Lithographic system



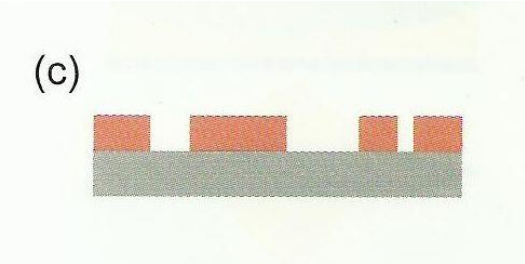
Illumination process

The resist is changed by the radiation

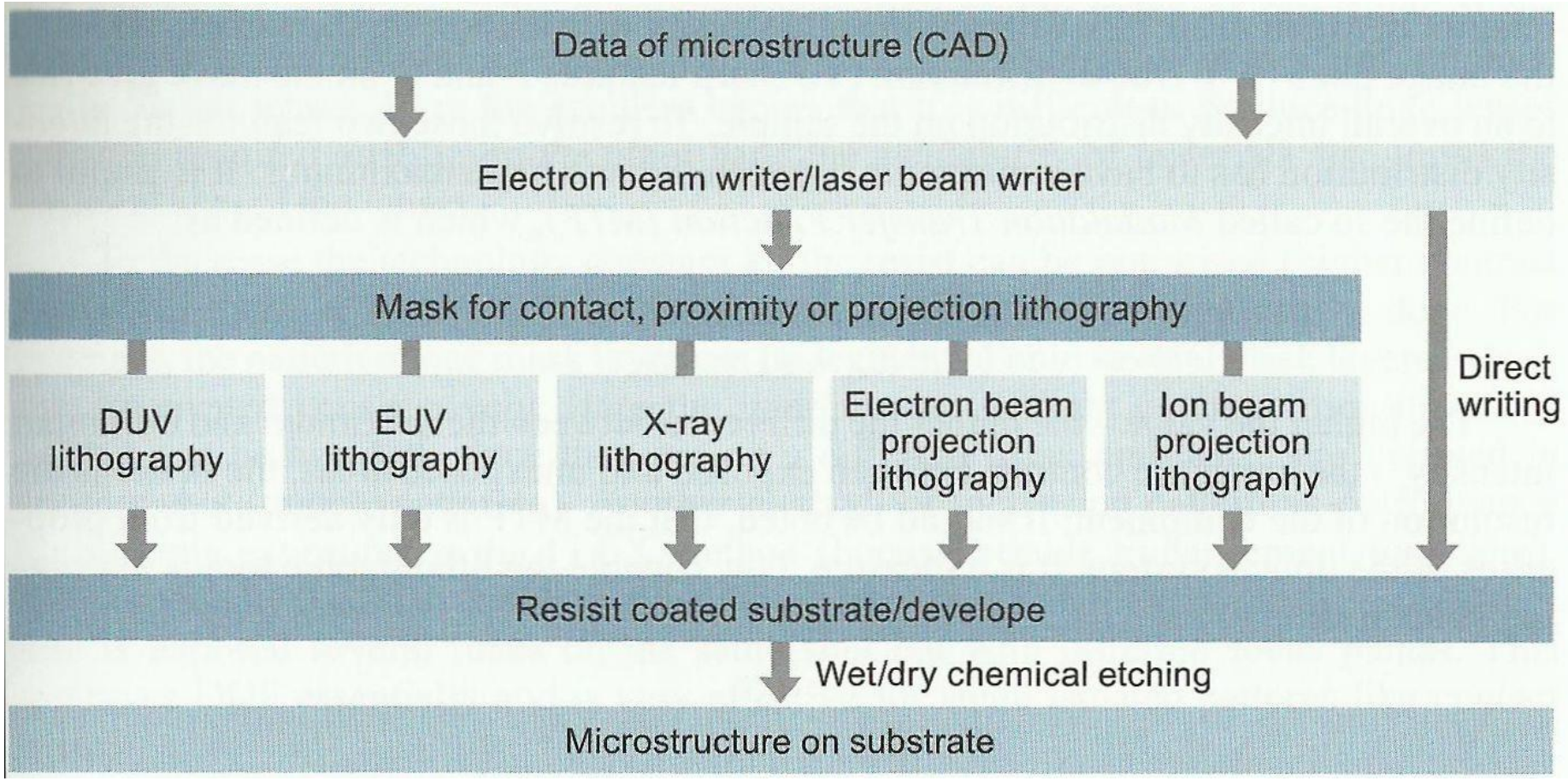


Development

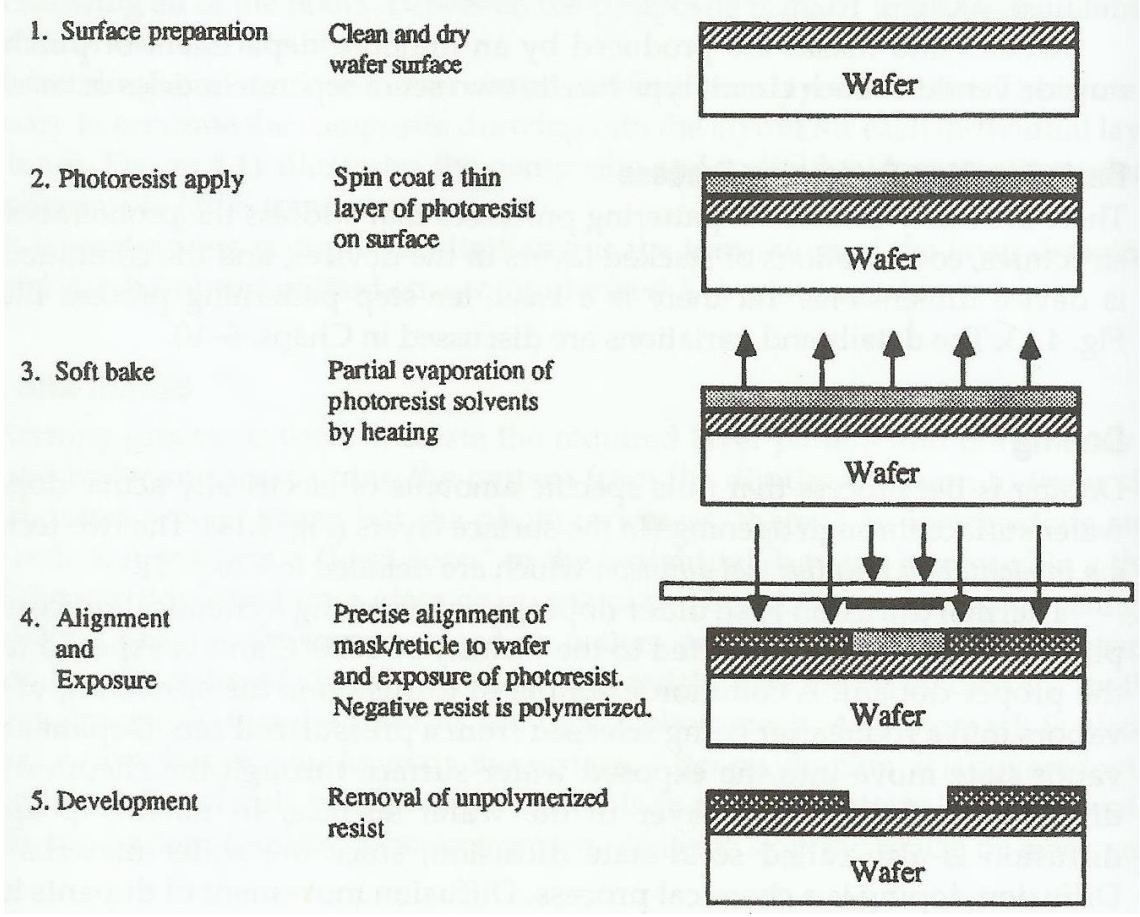
The illuminated resist can be etched selectively to the unexposed resist

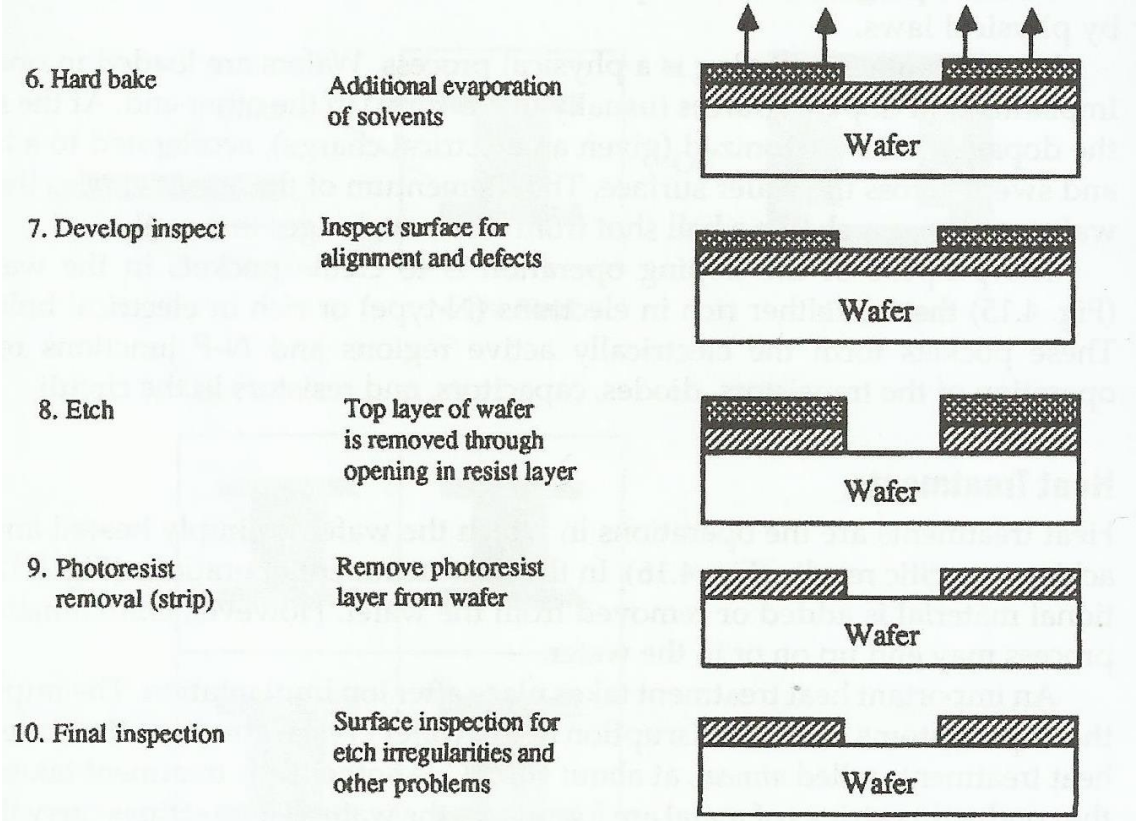


Lithographic classes



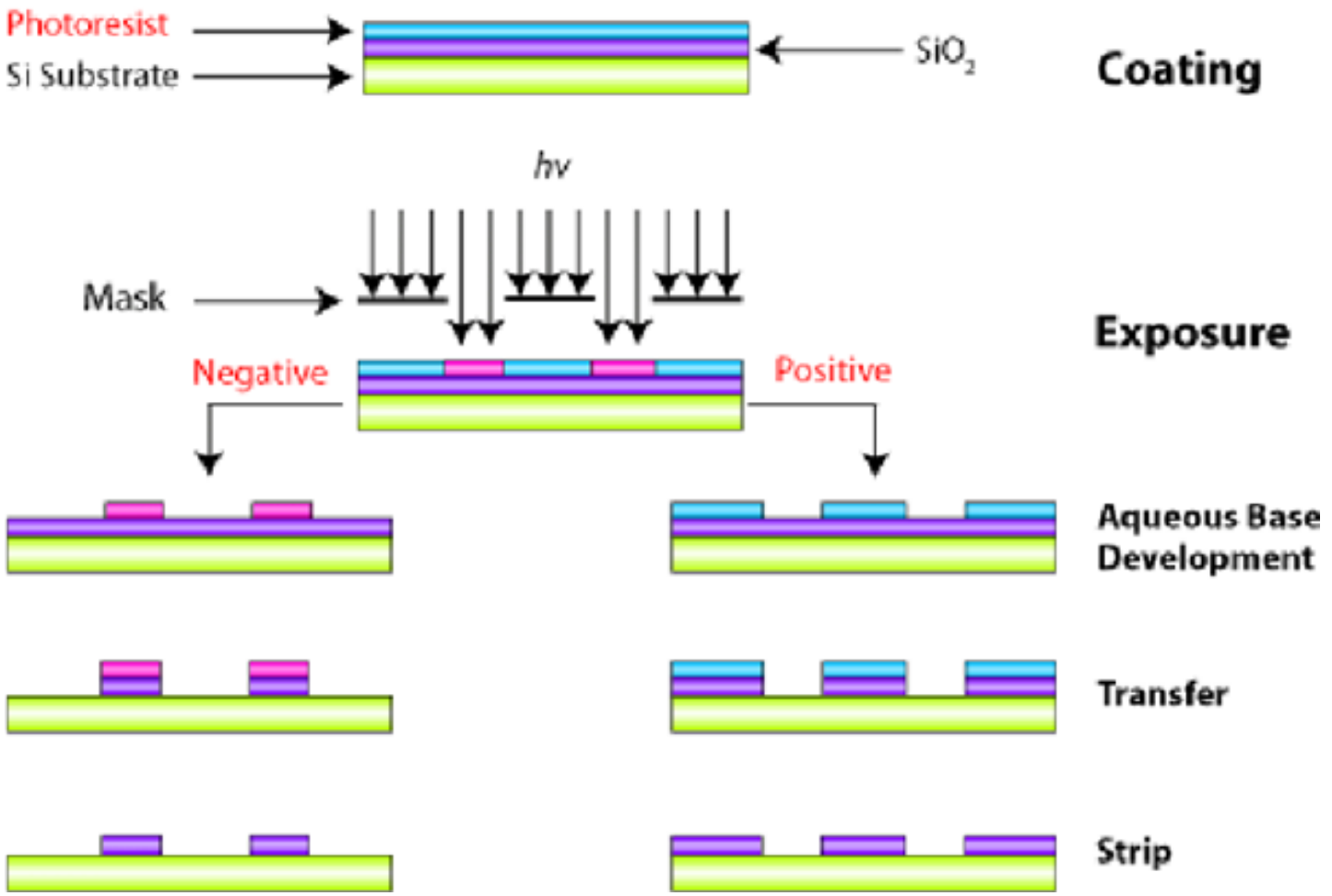
Classical 10-step photolithographic process





Photolithography for etching

In **negative** resist: photopolymerization

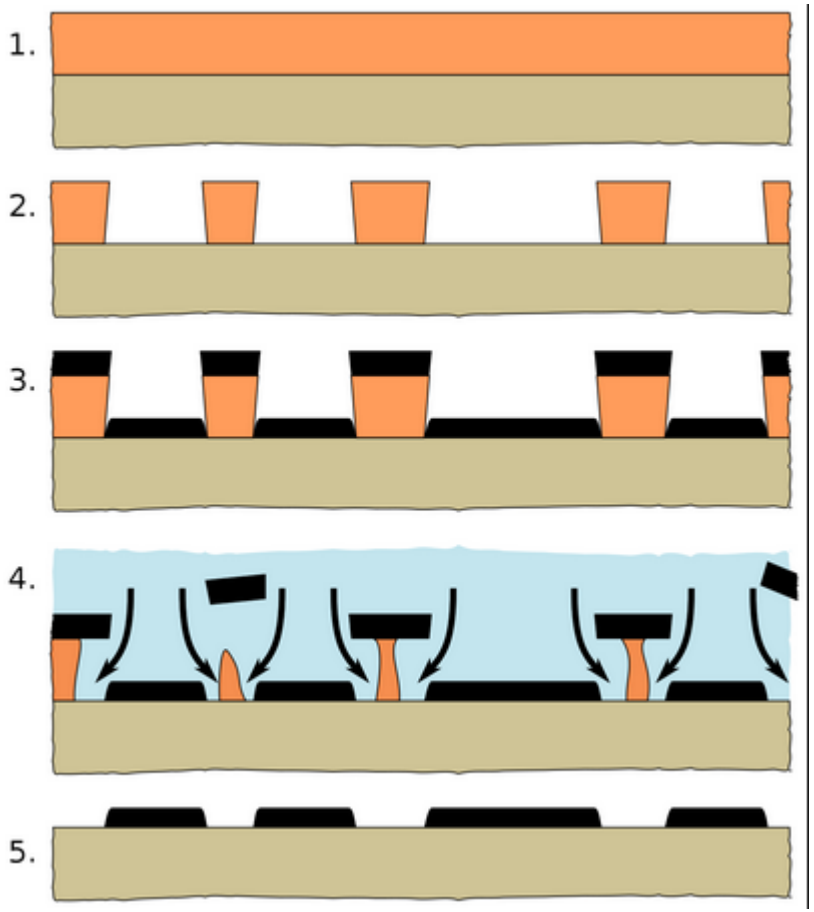


In **positive** resist: photosolubilization

Photolithography for lift-off

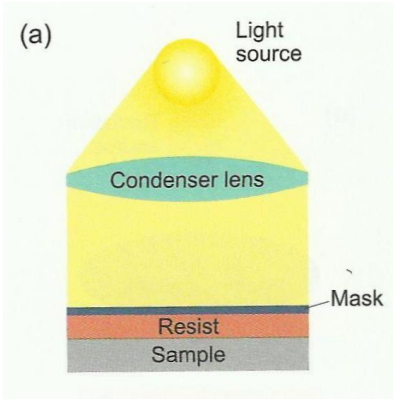
- A simple technique for metal pattern
- Wet technique with high risk of failure

  → not applied in mass production



Lithographic classes

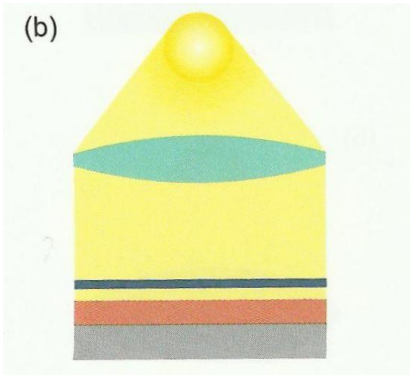
Contact



$$\mathrm{MFS} = \sqrt{d \cdot \lambda}$$

- Relatively low MFS
- Deterioration of the mask

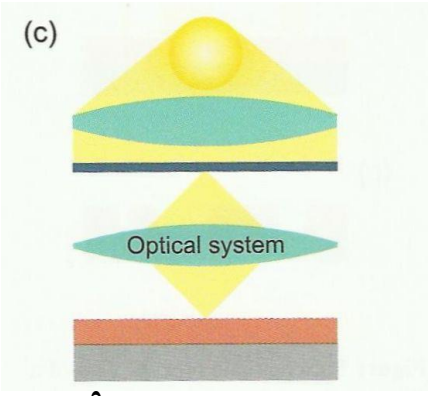
Proximity



$$\mathrm{MFS} = \sqrt{(d+g) \cdot \lambda}$$

- Higher MFS because of the gap
- No mask deterioration

Projection



$$\mathrm{MFS} = k_1 \frac{\lambda}{NA} \qquad DOF = k_2 \frac{n\lambda}{NA^2}$$

- Highest resolution, dominant in high-end production
- Slower process, expensive instrumentation

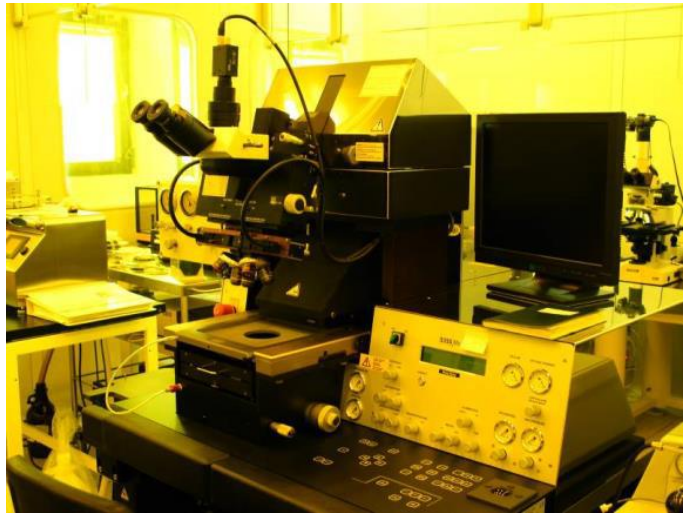
MFS:	Minimal Feauture Size
d:	thickness of the resist
λ:	wavelength
NA:	$= sin(\alpha) \cdot n$, numerical aperture
α:	half cone angle of illumination beam

DOF:	depth of focus
n:	refractive index of the medium between last optical element and substrate
k_1:	~0.4, 1st technology constant
k_2:	2nd technology constant

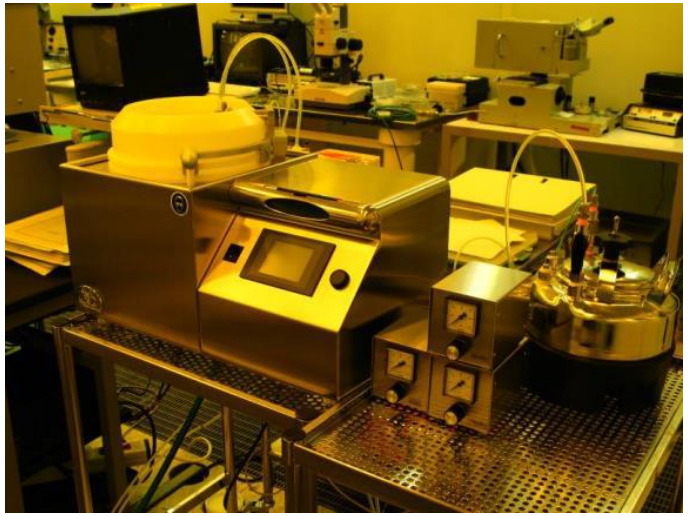
Typical contact photolithography tools

Spin-coater to cover the substrate with photoresist

Mask aligner to expose the photoresist through the mask



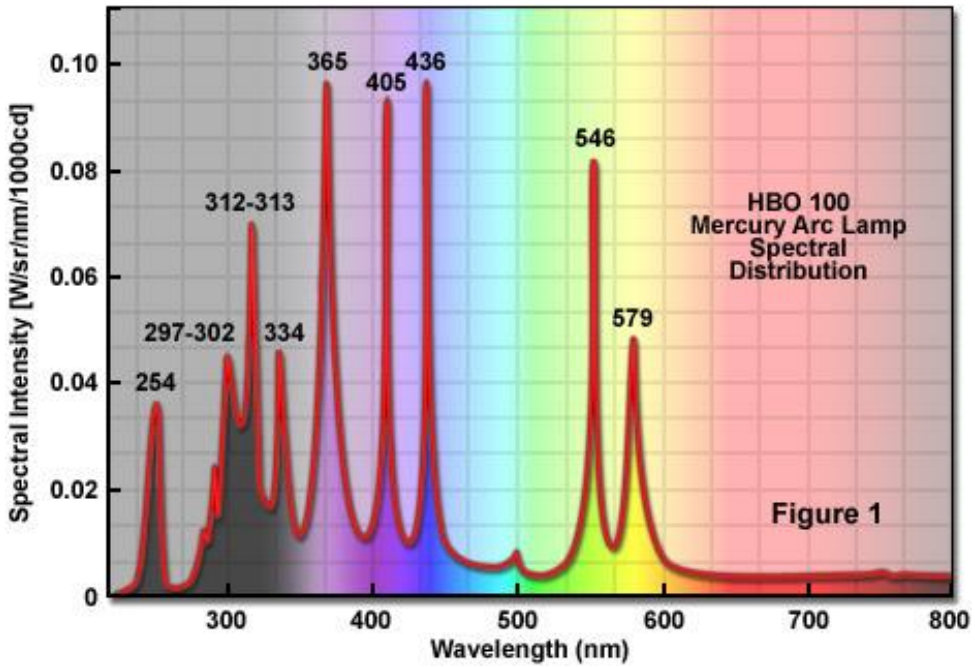
Developer to remove the exposed photoresist



Resolution enhancement: wavelength reduction

Source	Range	λ [nm]
Hg arc lamp	G-line, blue	436
Hg arc lamp	H-line, violet	405
Hg arc lamp	I-line, near UV	365
Hg/Xe arc lamp/KrF excimer laser	Deep UV (DUV)	248
ArF excimer laser	Deep UV (DUV)	193
Laser produced plasma; discharge produced plasma	Extreme UV (EUV)	13.5
X-ray tube, synchrotone	X-ray	~1

Spectrum of the Hg arc lamp



Vacuum UV (VUV): λ=10-200 nm; strong O_2 absorption λ <200 nm, while N_2 absorbs at λ <150 nm.

→ at deeper UV the instrumentation is getting more and more complicated and expensive.

Resolution enhancement in projection lithography

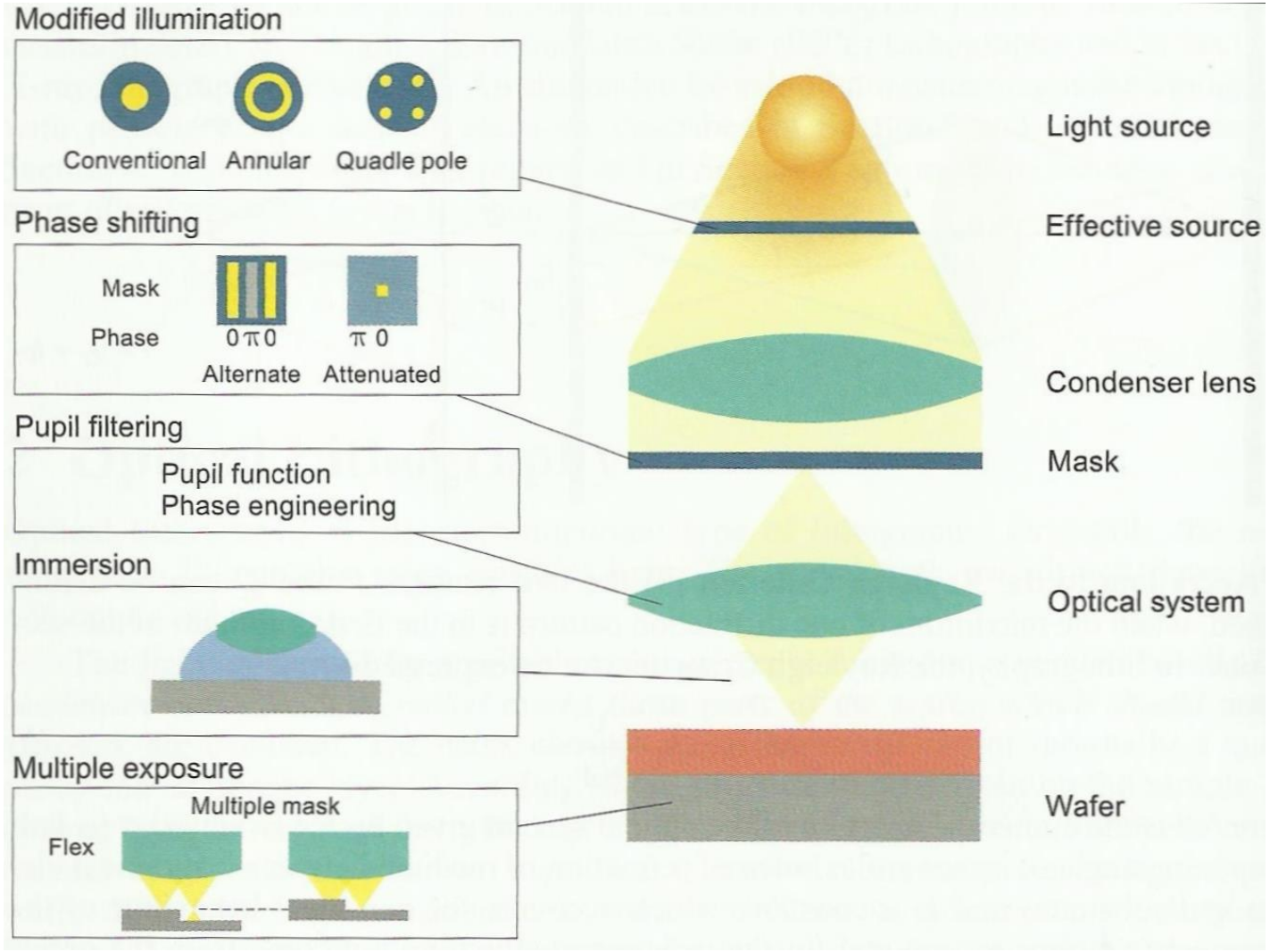
Introducing an aperture will generate an effective light source which results in an **off-axis illumination**

By an additional **phase shifting layer** on the mask the wavefront can be modified to utilize interference effect

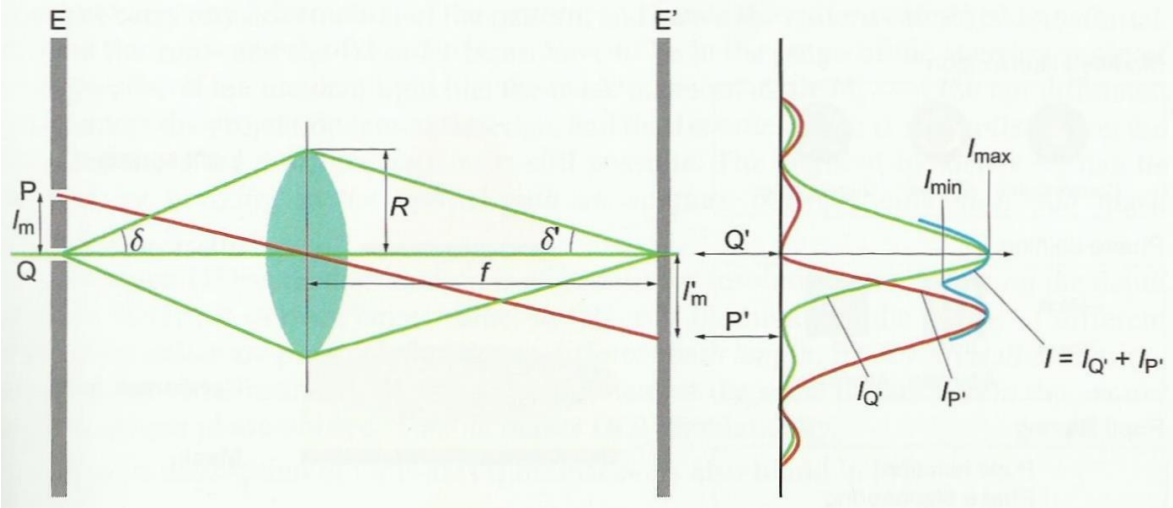
Blanking parts of the wave front after projection optics in **pupil filtering** also enhances the phase distribution on wafers

Immersium medium, like DI water (n=1,44) helps to **increase NA** up to ~1.2

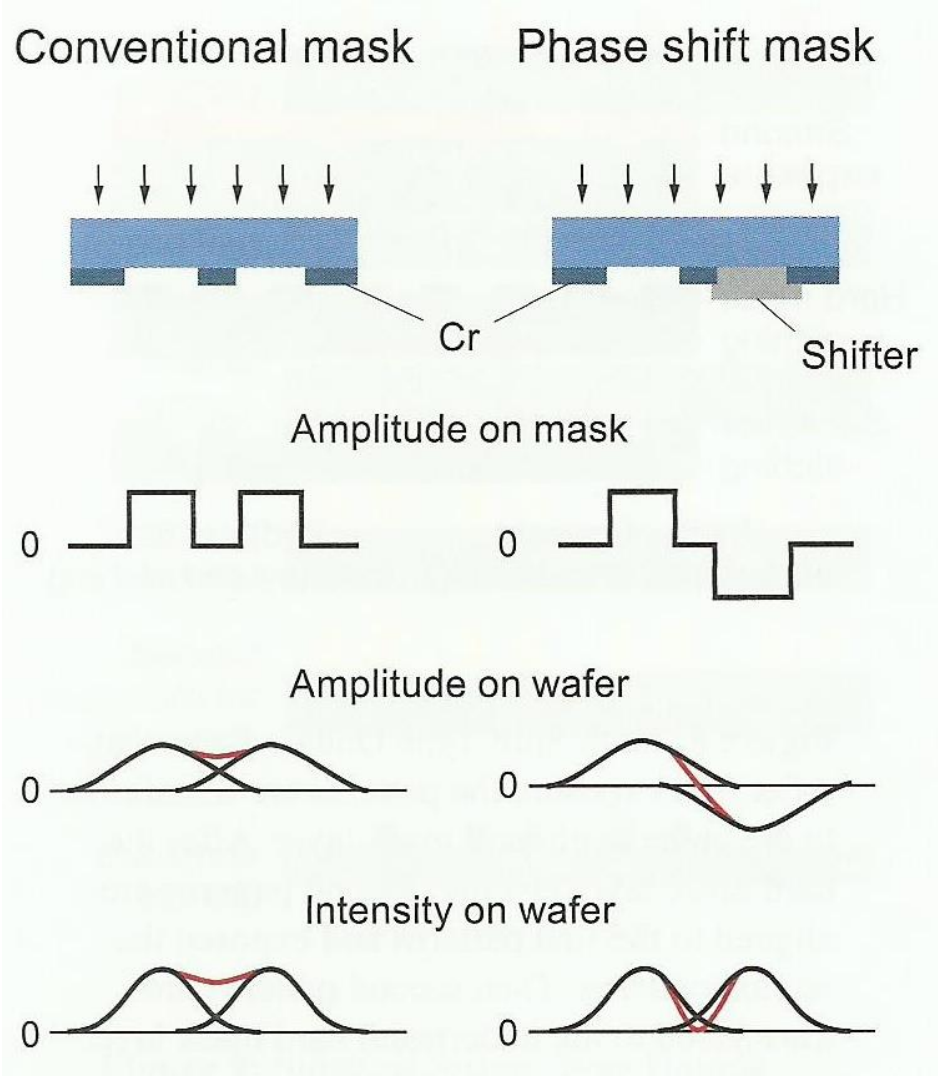
With **multiple exposures** of the same structure the patterns are optimized



Resolution enhancement by phase shifting technique



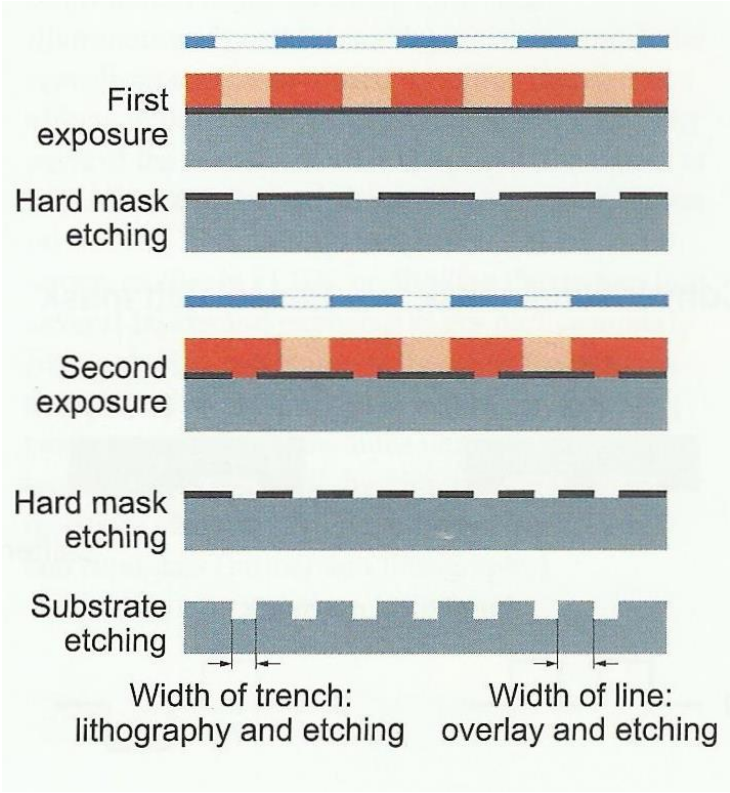
Modulation Transfer Function: $MTF = \dfrac{I_{max} - I_{min}}{I_{max} + I_{min}}$



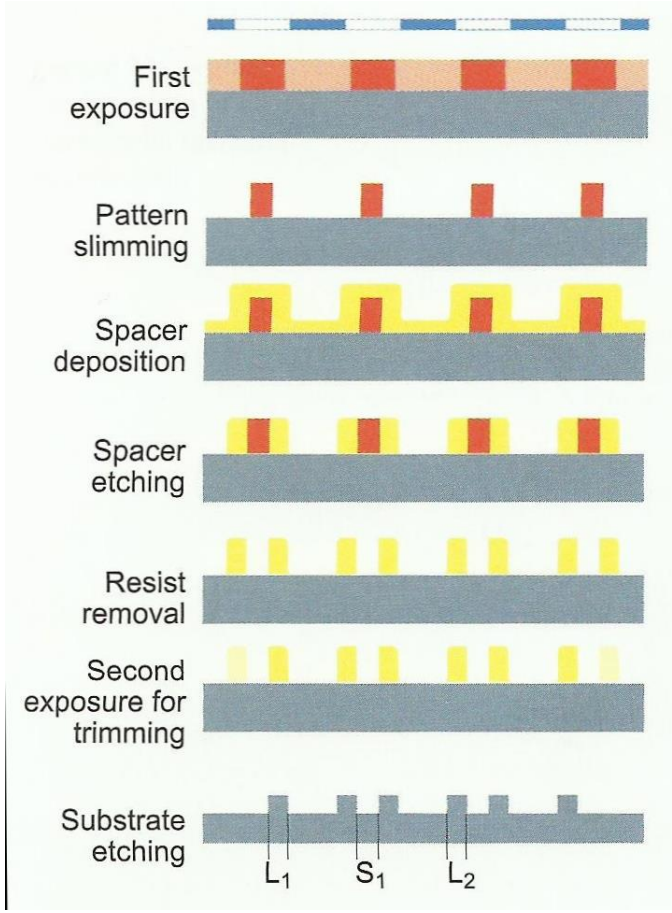
By an additional phase shifting layer we can benefit from the destructive interference.

Resolution enhancement by double patterning

Pitch split type double patterning

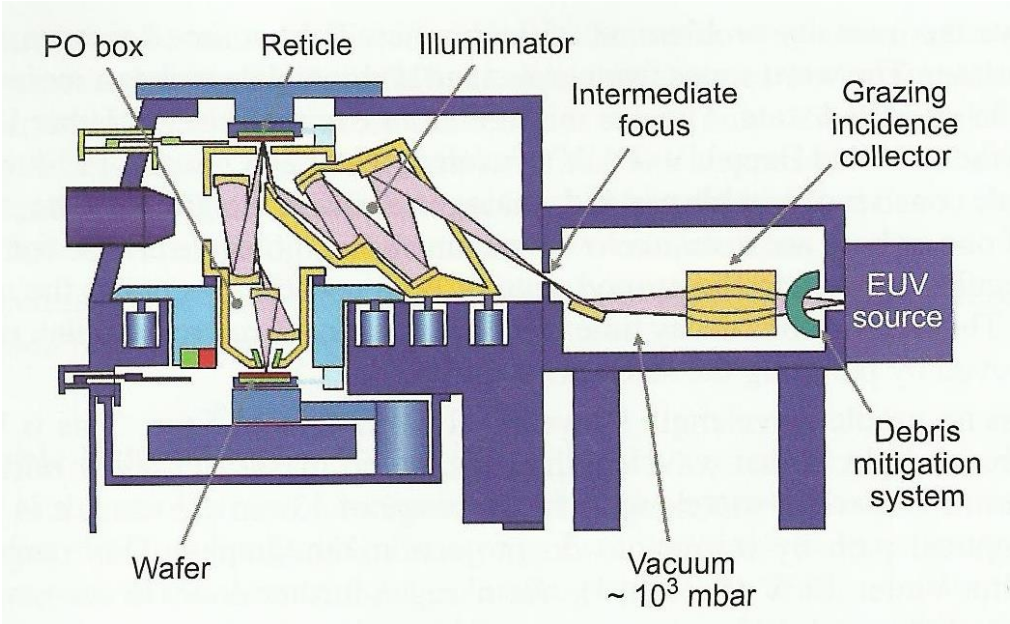


Sidewall spacer type double patterning

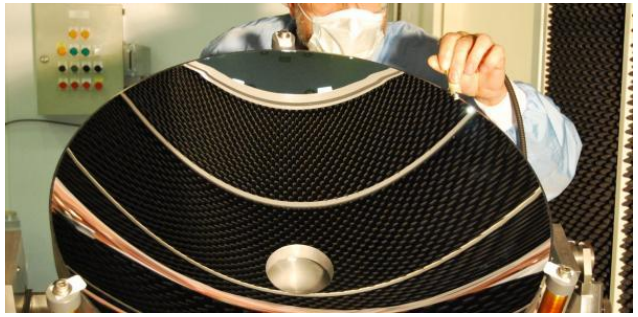


Extreme Ultraviolet (EUV) Lithography

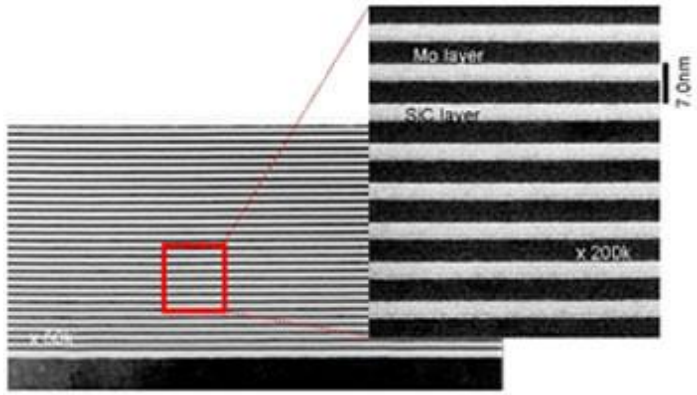
- Not only the wavelength the price is also extreme!
- Used for the 7-nm technology since 2019
- Because of the strong absorption of matters there is no lens in this range
- Instead multilayer (Bragg) mirrors are used with a limited reflectance of ~70%
- After 12 reflections I/I ~0.7^{12}=0.014 (only about 1%!)



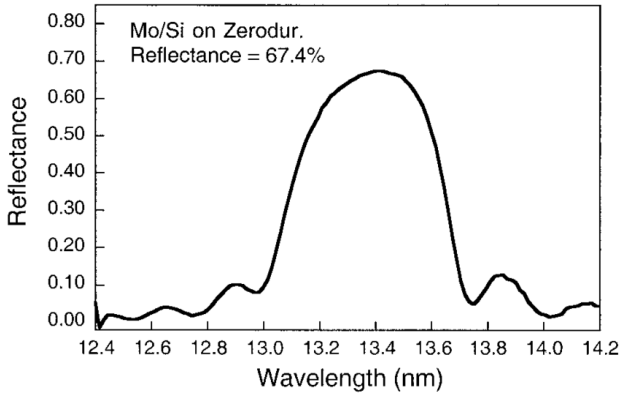
EUV spherical mirror with multilayer coating



Mo/SiC multilayer Bragg mirror



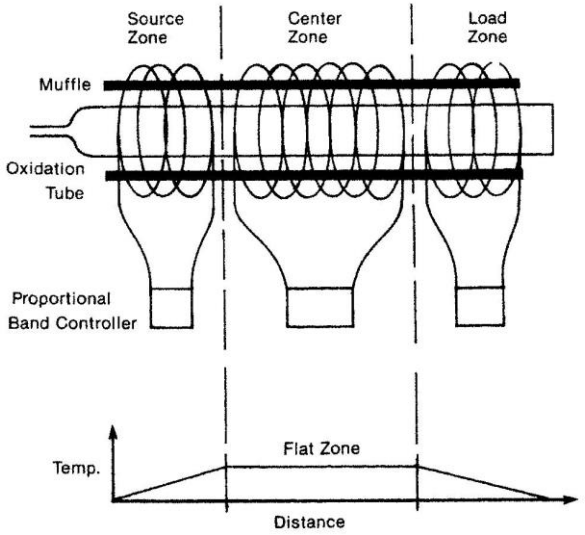
Reflectance of the mirror

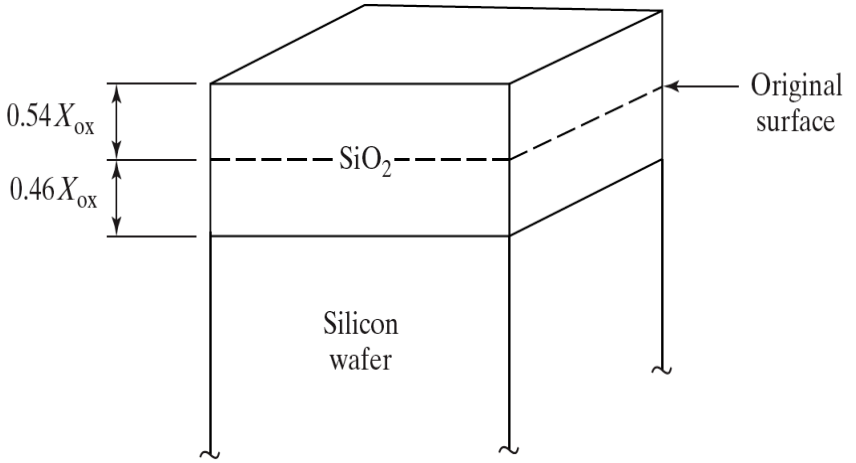


Thermal oxidation

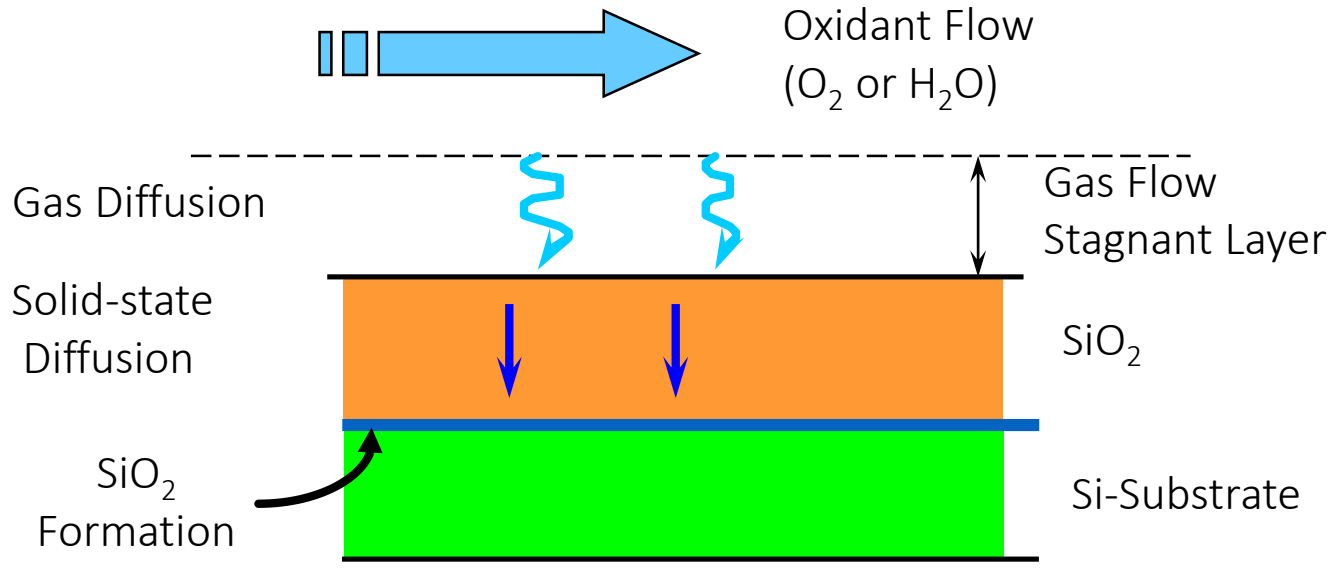
Thermal oxidation: technology

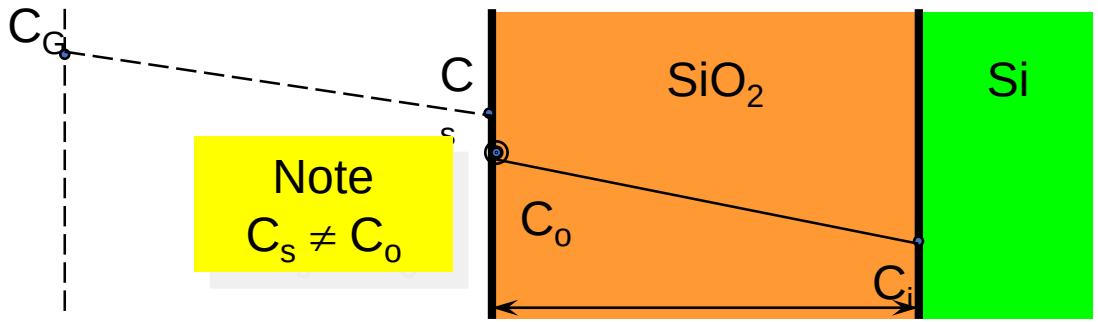
- Converts Si on the wafer into SiO_2 to obtain high quality insulator e,g. for ion implantation masking
- Annealing at a T=800-1200 °C in a quartz or SiC tube furnace using a movable quartz rack (boat)
- Atmosphere:
  - Water vapor (wet): $Si+2H_2O \rightarrow SiO_2+2H_{2\ (g)}$ (higher growth rate)
  - O_2 (dry): $Si+O_2 \rightarrow SiO_2$ (better quality)
- Growth occurs 54% above and 46% below the original surface as Si is consumed $X_{Si} = X_{ox}\frac{N_{ox}}{N_{Si}} = 0.46X_{ox}$





Thermal oxidation: growth kinetics





Thermal oxidation: growth kinetics

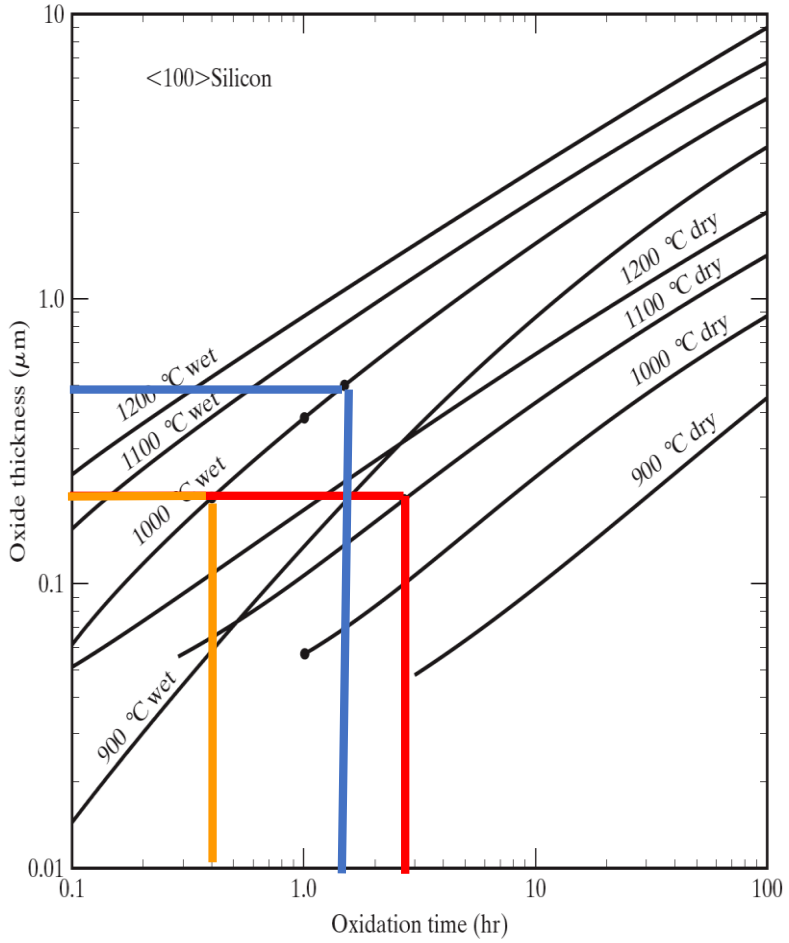
Example:

A <100> silicon wafer has a 2000-Å oxide on its surface

(a) How long did it take to grow this oxide at 1100^{o} C in dry oxygen?

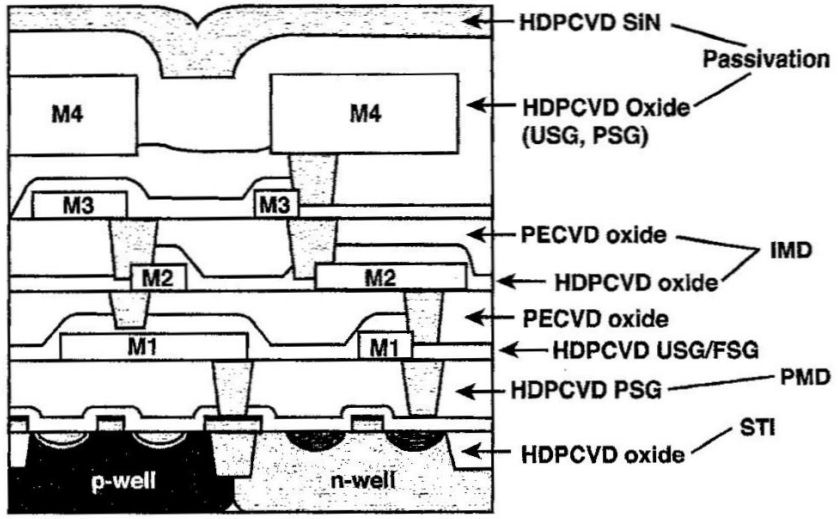
(b)The wafer is put back in the furnace in wet oxygen at 1000^{o} C. How long will it take to grow an additional 3000 Å of oxide?

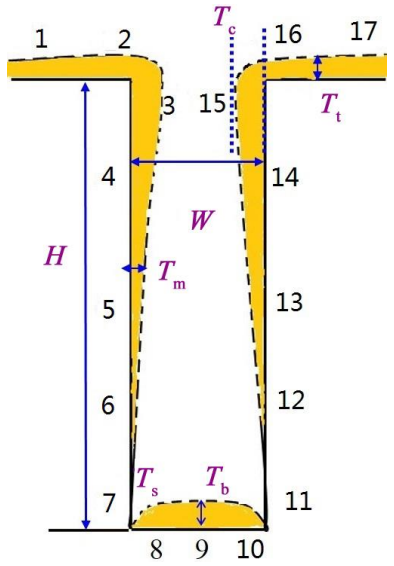
Thermal oxidation on <100> Si



Thin film deposition

CMOS materials





Non-uniformity in deep trenches; aspect ratio (depth/width) plays an important role

Film parameters

- Thickness/uniformity → well-controlled thickness over the wafer; trenches are challenging
- Surface flatness/roughness → can influence the subsequent layer
- Composition/grain size → stoichometry is important; grain size will effect the electrical/mechanical properties
- Internal stress → have to be stress-free to avoid cracking accompanied often by contamination or short cut
- Purity → excluding mobile ions or oxygen from epitaxial layers
- Electrical properties → metals with high conductivity, low-k dielectrics, high-k dielectrics etc

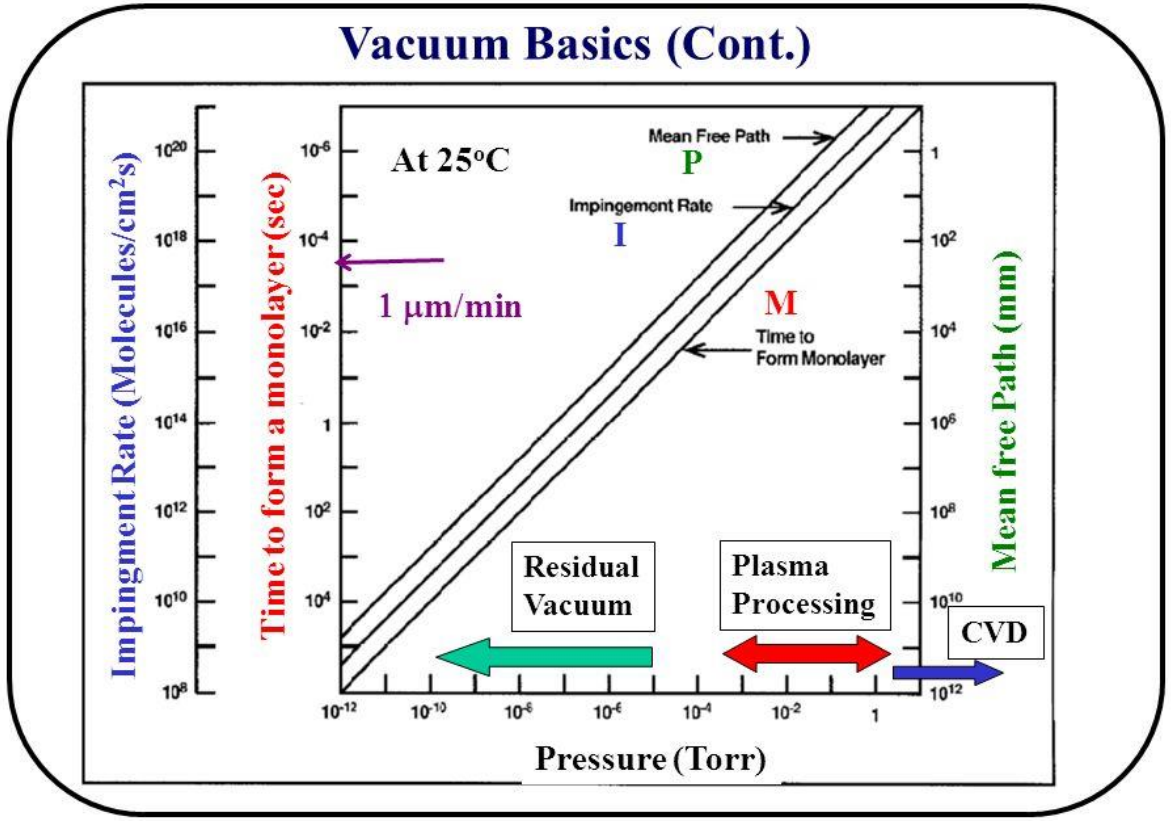
Film deposition methods: categories

- In CVD, the wafer is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposit.
- PVD is a process in which the material goes from a condensed phase to a vapor phase and then back to a thin film condensed phase.

	Chemical Vapor Deposition (CVD)	**Physical Vapor Deposition (PVD)**		
	LPCVD, MOCVD etc.	Evaporation /Molecular Beam Epitaxy	Sputtering	Pulsed Laser Deposition (PLD)
Production mechanism of depositing species	Chemical reaction	Thermal energy	Momentum transfer	Thermal energy
Deposition rate	Low, moderate	High, up to 75 nm/min	Low, moderate	Moderate
Deposition Species	Precursor molecules	Atoms and ions	Atoms and ions	Atom, ions, clusters
Energy of deposited species	Low, can be high with plasma-aid	Low, 0.1-0.5 eV	Can be high, 1-100 eV	Low to high
Scalable to wafer size	Up to large	Up to large	Up to large	limited

Film deposition methods: gas kinetics

Using Maxwell velocity distribution: $\lambda = \frac{1}{\sqrt{2\pi}\, N d^2} = \frac{k_B T}{\sqrt{2\pi}\, p d^2}$

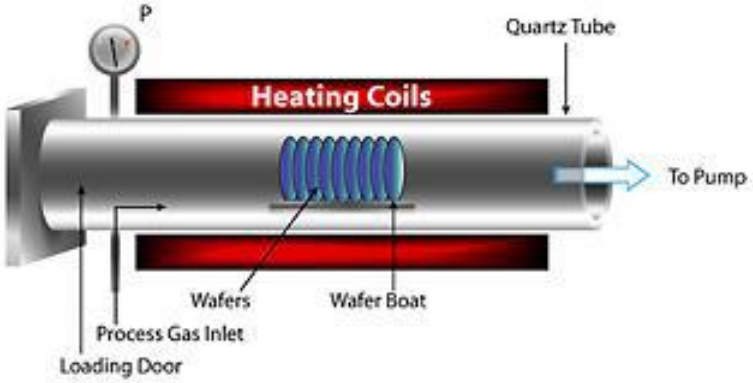


Chemical vapor deposition (CVD)

- Wafer is exposed to one or more volatile precursor which react and/or decompose on the substrate surface to produce high quality thin film
- Volatile by-products are removed by gas flow through the reaction chamber
- Materials in various forms: epitaxial, polycrystalline, amorphous
- Materials: Si, SiO_2, SiC, Si_xN, SiON, W, high-k dielectrics, low-k dielectrics
- High quality, conformal deposition (high step coverage)
- For example:

poli Si at 580-650 °C and ~1 mbar: $SiH_4 \Leftrightarrow Si(s) + 2H_2$

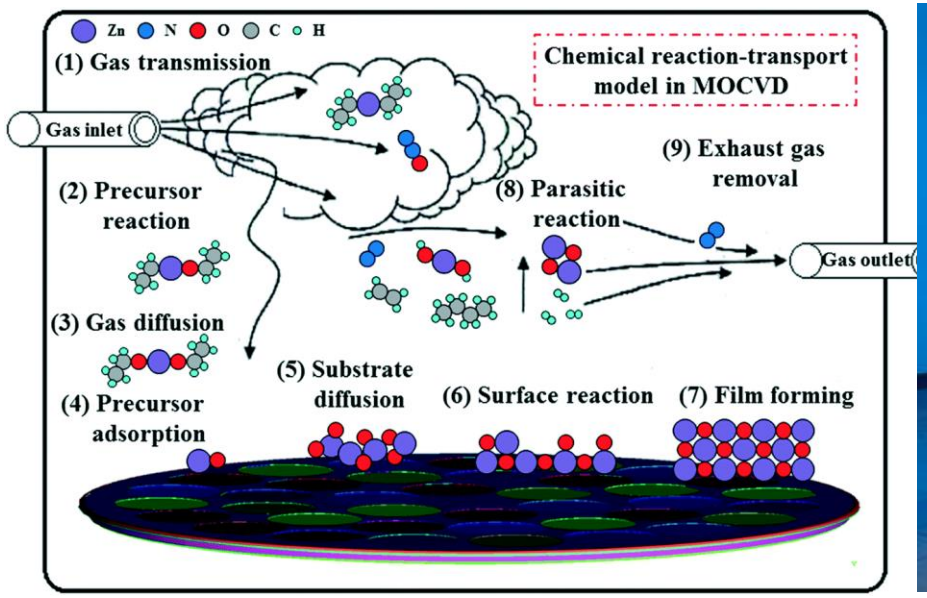
Si_3N_4 at 700-900 °C and atm. Pr.: $3SiH_4+4NH_3 \Leftrightarrow Si_3N_4(s) + 12\ H_2$



Chemical vapor deposition (CVD)

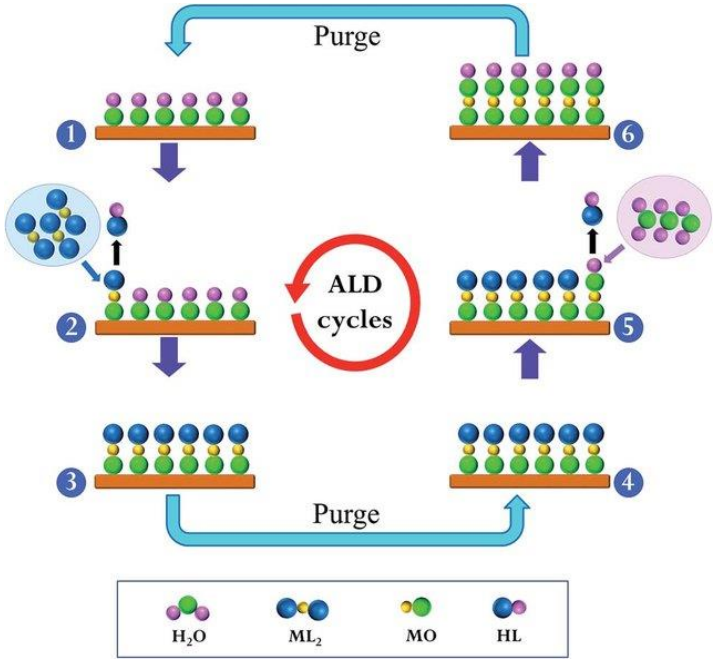
Several subcategories and reactor designs:

- By operation conditions: atmospheric, low-pressure (LPCVD), ultrahigh vacuum
- Plasma methods: plasma-enhanced (PECVD), remote plasma enhanced (RPCVD)
- By the precursor: e.g. metalorganic chemical vapor deposition (MOCVD)



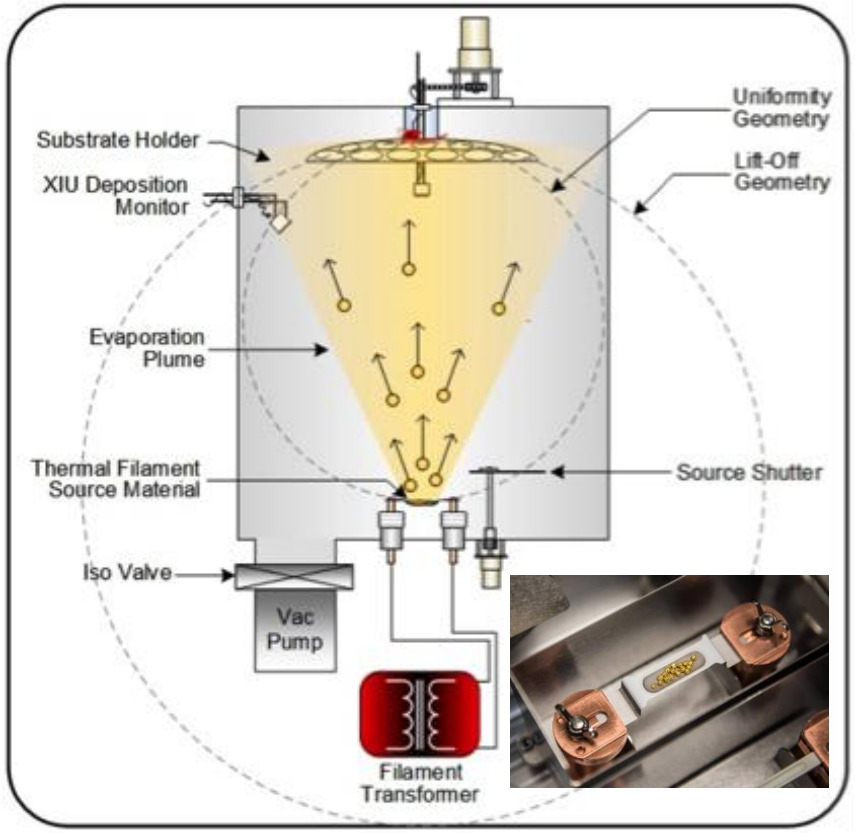
Atomic Layer Deposition (ALD)

- A subclass of chemical vapor deposition based on subsequential use of gas phase chemical process
- Two precursors react with the surface of the material one at a time in a sequential, self-limiting manner
- Atomic control of the layers, but slow growing rate
- Both metals and (high-k) dielectrics; key method in the fabrication of semiconductor devices
- Main setting parameters: substrate temperature, pulse times for precursors and purging, temperature of the precursor container
- Plasma assisted mode is also possible



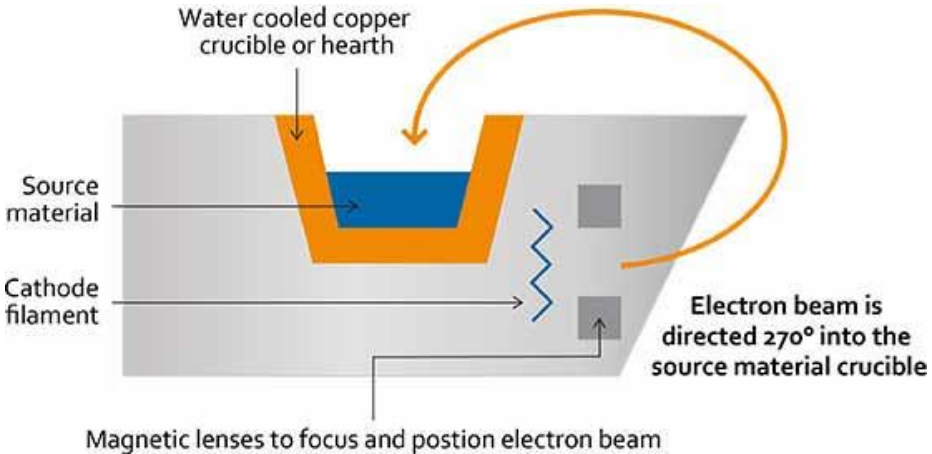
Evaporation type PVD

- Heating of a solid material inside a high vacuum chamber, taking it to a temperature which produces some vapor pressure (often melting)
- Since E_{kin}<1 eV $\rightarrow$ High vacuum is needed ($< 10^{-4}$ Torr) for $\lambda \gg D_{source\text{-}substrate}$
- Directional material transfer: vapor stream traversing the chamber and hitting the substrate (for uniform layer: planetary movement of the wafers, for lift-off process: fix sample position)
- Heating of the source: resistive and e-beam evaporation
- In thermal evaporation: resistively heating element (~50-100 A, ~6-20 V) made of a refractory material (boat or filament)
- Most system use Quartz Crystal Microbalance for real-time monitoring of deposition rate (S~μg/cm^2)



PVD1: Electron beam evaporation

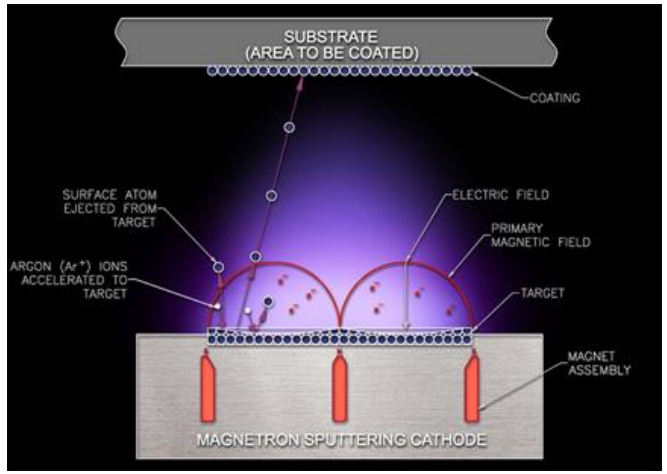
- E-beam evaporator uses an electron beam to heat up source material to vapor phase
- E-beam is magnetically directed (270°) into the crucible of the source material
- Very high power density: ~ 10 kV, ~ 0.1A, ~1 kW absorbed in a small volume
- Water cooled container
- Programmed e-beam scanning for the uniform usage of the source
- Several material can be deposited using multiple crucible
- More developed than thermal evaporation. Benefits:
  - Less contamination from the crucible material
  - Very high deposition rate
  - High material utilization efficiency



Linear pocket e-beam source

PVD2: Sputtering

- A kind of physical vapor deposition (PVD) process for thin films
- Particles are ejected from the solid target due to ion bombardment
- Due to higher kinetic energy, better adhesion to the substrate than in case of vacuum evaporation
- Done either using DC voltage (DC sputtering) or AC voltage (13,56 MHz, RF sputtering)
- Metals can be deposited by DC or pulsed DC
- Insulators can be deposited either from ceramic target by RF or from metallic target in reactive atmosphere (e.g. AlN from Al in N_2 atmosphere)
- Can be combined with e-beam evaporators



Combined PVD-CVD cluster systems

- Automatic deposition of subsequent layers without breaking the vacuum during the process

Etching process

Etching techniques

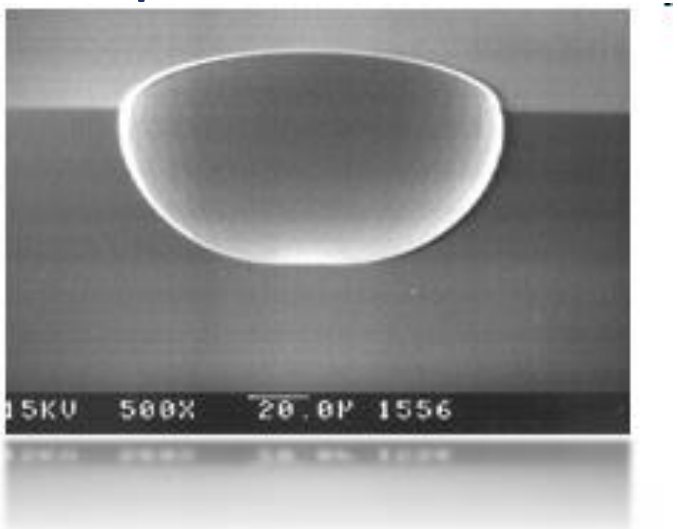
Wet etching

- Liquid etchant
- Chemical reaction
- High selectivity

Dry etching

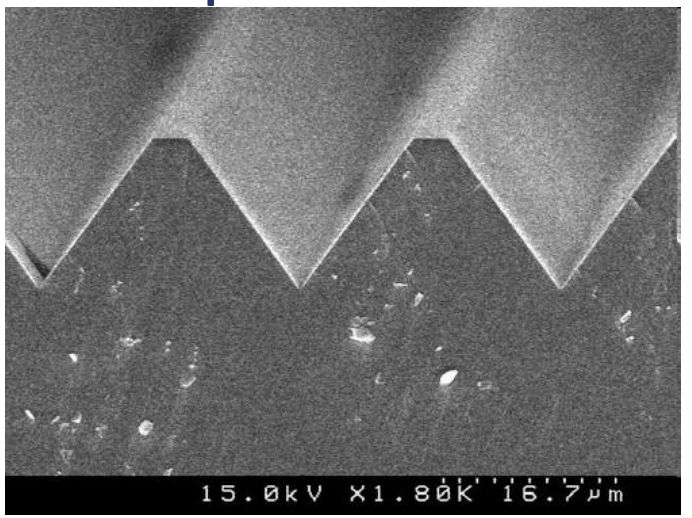
- Vapor phase etchants
- Chemical and physical processes
- Lower selectivity

Isotropic



E.g. HF-HNO_3-CH_3COOH (polishing etchant): etching rate is not direction dependent

Anisotropic



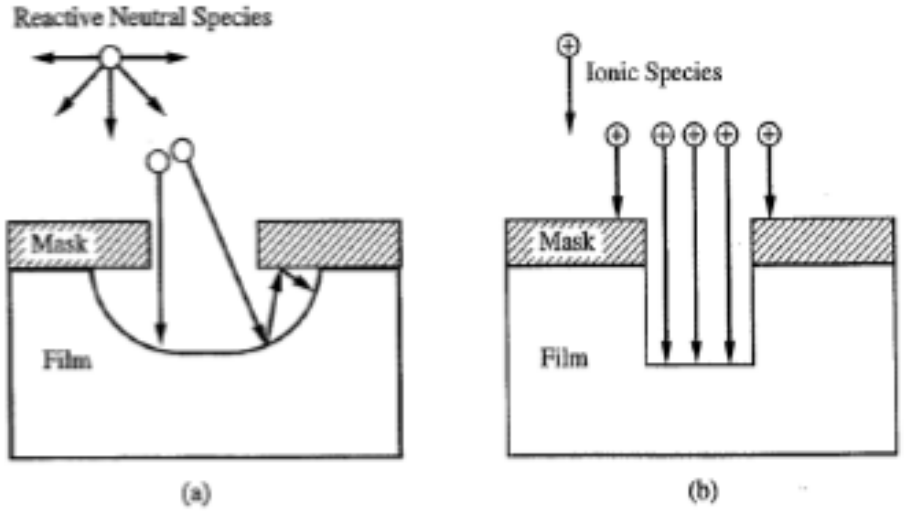
E.g. KOH etch: Etching rate depends on the crystal faces

Dry etching

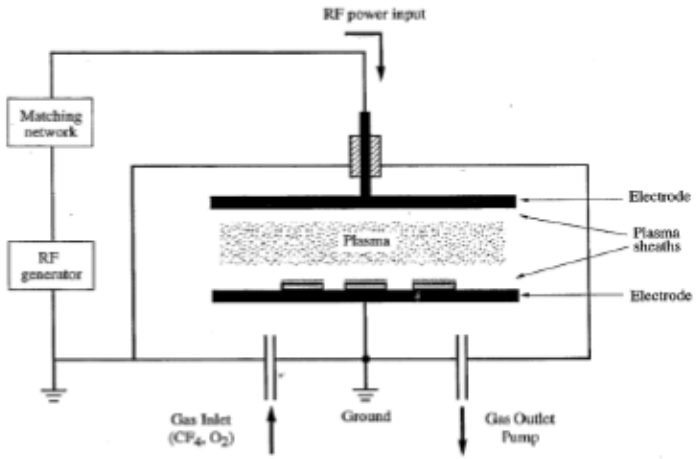
- More efficient **chemical** etching using reactive radicals (e.g. atomic F) (Plasma etching)
  - $CF_4+e^- \rightarrow CF_3+F+e^-$
  - $4F+Si \rightarrow SiF_4$
- More anisotropic **physical** etching by charged particles (Ion milling)

operations are often combined:
Reactive Ion Etching (RIE)

Reactive vs. phyisical ion etching

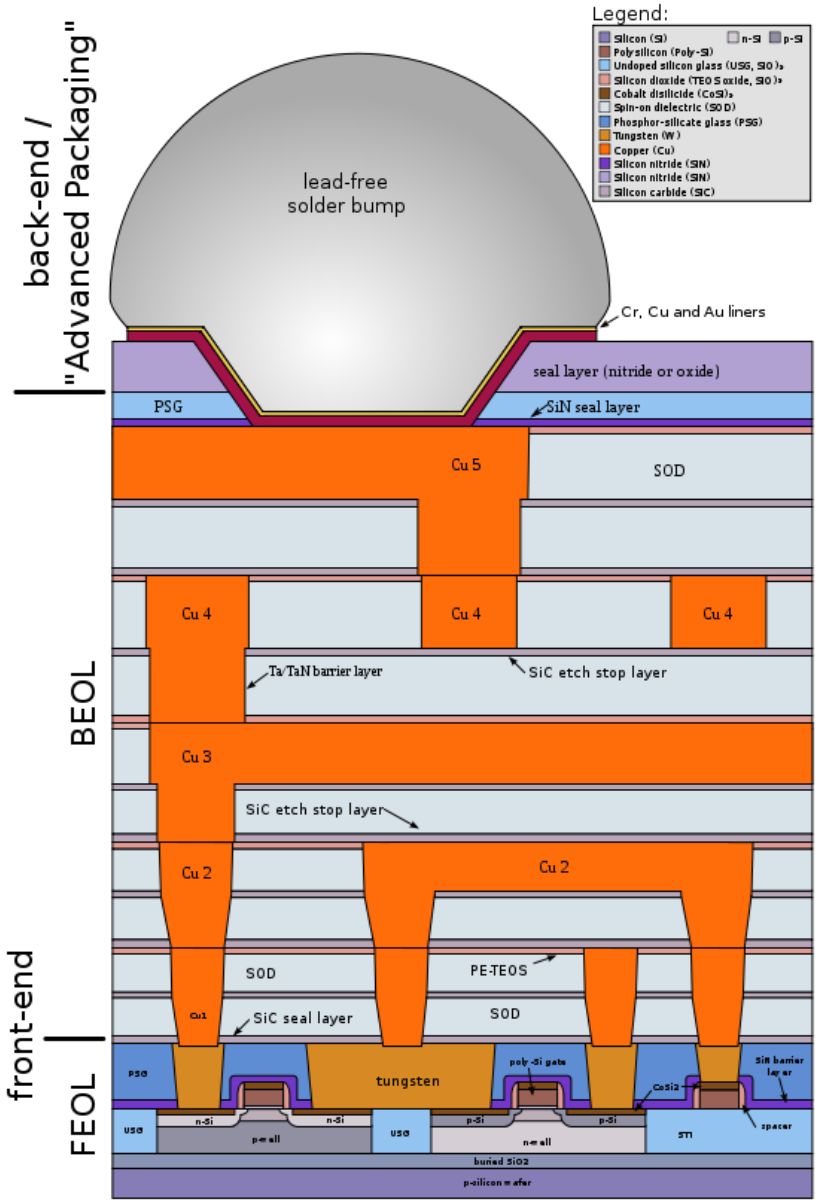


Planar plasma etcher



Interconnection metalization

Back-end of the line (BEOL) interconnections



- Traditional IC connectors are made of Al
- Lower resistivity is needed to improve the performance (lower Joule heating, higher current density)
- Challenge with Cu patterning; doesn't produce volatile byproduct
- Solution: **Damascene process** (introduced by IBM in the 1990s)

Damascene gold plate

Damascene process

Instead of etching the metal via photolithography pattern, gaps in low-k dielectric are filled by PVD seed layer and electroplated Cu.

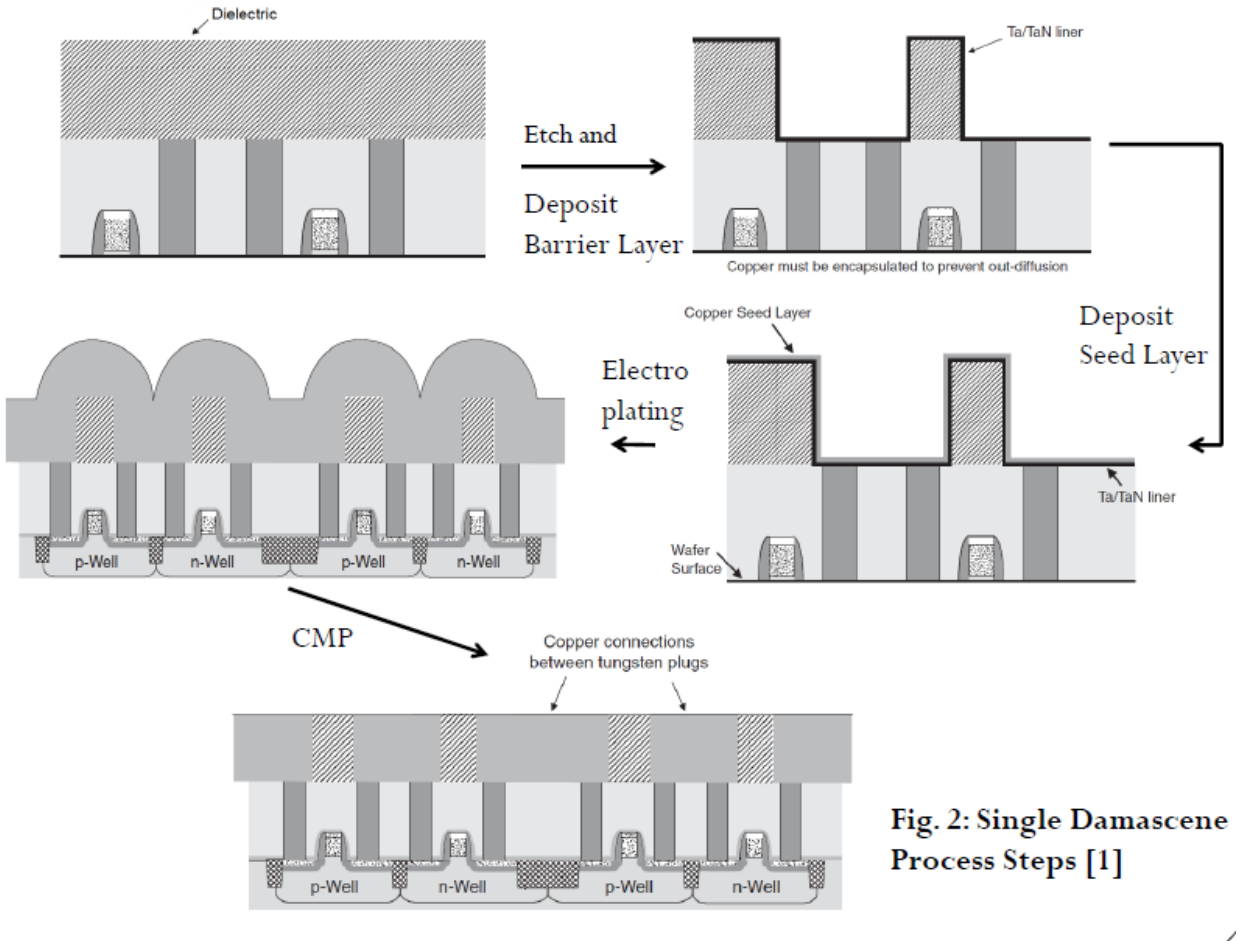
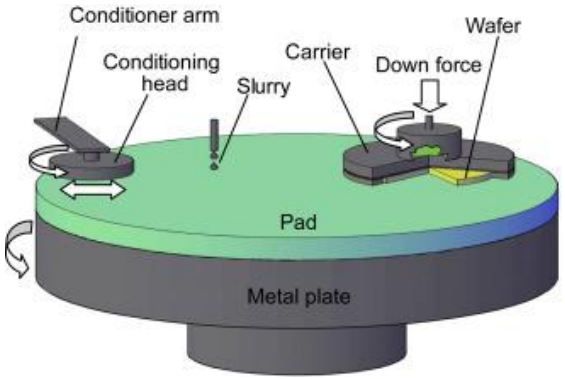
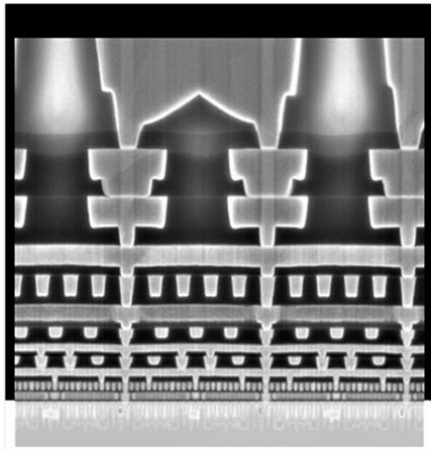


Fig. 2: Single Damascene Process Steps [1]

Chemical mechanical polishing



State-of-the-art SRAM



Video