ADVANCED SEMICONDUCTOR DEVICES

02_CMOS_Technology

February 12nd, 19th, 2020
Stages of semiconductor manufacturing

- **Material preparation:** Sand to polycrystalline silicon
- **Crystal growth and wafer preparation:** Polycrystalline silicon to wafer
- **Wafer fabrication**
  Circuit/devices formed in/on wafer surface
- **Packaging**
  Functioning die placed in a protective package
Si single crystal

High quality single crystal in large size

Single crystal Si grown by Czochralski method

Face centered cubic crystal (fcc)

+ advantageous physical properties and good quality native oxide

- Microelectronics is based on mainly on Si.
- III-V semiconductors play an important role in optoelectronics.
Czochralski method

- Polysilicon nuggets with the dopants are melted in the quartz crucible at a $T>1400^\circ\text{C}$
- Purity of the polysilicon nuggets 99.9999999% (9N)
- Si crystal Si crystal with the desired orientation ($<100>$, $<110>$, $<111>$) is slowly pulled out; both the seed and the crucible is rotated to maintain homogeneity
- Typical impurity concentration: $N_O: 10^{18}\ \text{cm}^{-3}$, $N_C: 10^{16}\ \text{cm}^{-3}$ ($N_{Si}=5\cdot10^{22}\ \text{1/cm}^3$)
Floating zone method

- No vessel is needed → higher purity than for CZ
- Carrier concentration down to $10^{11} \text{ cm}^{-3}$ → highly resistive wafers (1-10 kOhm·cm)
- Max diameter is 150 mm because of the surface tension limitation
- Evacuated chamber or filled with inert gas
- Molten zone carries the impurities away from the c-Si → reduces impurity concentration (most impurities are more soluble in the melt than the crystal)
- Higher price compared to CZ
- Doping by dopant gases, such as PH$_3$, AsH$_3$, B$_2$H$_6$
- Mainly used for power devices
Wafer processing

Annular saw

- Wafer surface is relatively smooth, subsequent steps take less time
- Low throughput

Wire saw

- Wafer surface is less smooth, subsequent lapping takes more time
- High throughput

The process is continued and finished by lapping, etching, polishing and cleaning
Wafer doping

The diagram illustrates the relationship between dopant density and resistivity for n-Si (phosphorous) and p-Si (boron) materials. The x-axis represents dopant density in/cm^3, while the y-axis shows resistivity in ohm cm. The red line represents n-Si (phosphorous), and the blue line represents p-Si (boron).
# Si wafer specification

<table>
<thead>
<tr>
<th>Diameter (mm)</th>
<th>Growth</th>
<th>Dopant</th>
<th>Orientation</th>
<th>Finish</th>
<th>Coating</th>
</tr>
</thead>
<tbody>
<tr>
<td>50.8</td>
<td>CZ</td>
<td>B</td>
<td>&lt;100&gt;</td>
<td>Single Side</td>
<td>With</td>
</tr>
<tr>
<td>76.2</td>
<td>CZ</td>
<td>Ph</td>
<td>&lt;110&gt;</td>
<td>Double Side</td>
<td>Without</td>
</tr>
<tr>
<td>100</td>
<td>CZ</td>
<td>Sb</td>
<td>&lt;100&gt;</td>
<td>As Cut</td>
<td>With</td>
</tr>
<tr>
<td>125</td>
<td>CZ</td>
<td>As</td>
<td>&lt;111&gt;</td>
<td>As Lapped</td>
<td>Without</td>
</tr>
<tr>
<td>150</td>
<td>CZ</td>
<td>Undoped</td>
<td>&lt;111&gt;</td>
<td>Ground</td>
<td>Without</td>
</tr>
<tr>
<td>200</td>
<td>CZ</td>
<td>Intrinsic</td>
<td>&lt;110&gt;</td>
<td>Etched</td>
<td>Without</td>
</tr>
<tr>
<td>300</td>
<td>CZ</td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>TTV</th>
<th>Bow</th>
<th>Warp</th>
<th>Thickness</th>
<th>Resistivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>≤</td>
<td>≤</td>
<td>≤</td>
<td>min ≥</td>
<td>min ≥</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>max ≤</td>
<td>max ≤</td>
</tr>
</tbody>
</table>

![12" Si wafer (300 mm)](image)
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- **Packaging**
  - Functioning die placed in a protective package
### Wafer/chip processing techniques

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<th>III) Subtractive methods</th>
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<td><strong>Thin film deposition</strong></td>
<td><strong>Etching</strong></td>
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<td>• Implantation</td>
<td>• Chemical Vapor Deposition (CVD)</td>
<td>• Wet chemical etching</td>
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<td>• Amorphization</td>
<td>• Physical Vapor Deposition (PVD)</td>
<td>• Ion beam etching</td>
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<tr>
<td>• Smart-cut</td>
<td>• Chemical solution deposition (CSD)</td>
<td>• Reactive Ion Etching</td>
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<td>• (Thermal growth)</td>
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<tr>
<td><strong>Radiative treatment</strong></td>
<td><strong>Printing techniques</strong></td>
<td><strong>Tool-Assisted Material Removal</strong></td>
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<td>• Resist exposure</td>
<td>• Ink-jet printing</td>
<td>• Chemical-mechanical polishing (CMP)</td>
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<td>• Polymer hardening</td>
<td>• Microcontact printing</td>
<td>• Chipping</td>
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<td>• Drilling</td>
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<td><strong>Thermal annealing</strong></td>
<td><strong>Assembly</strong></td>
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<tr>
<td>• Crystallization</td>
<td>• Wafer bonding</td>
<td></td>
</tr>
<tr>
<td>• Diffusion</td>
<td>• Surface mount technology</td>
<td></td>
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<tr>
<td>• Change of phase</td>
<td>• Wiring and bonding methods</td>
<td></td>
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<tr>
<td>• (Thermal growth)</td>
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</table>
CMOS fabrication process

- Si wafer manufacturing
- Thermal oxidation
- Doping by ion implantation
- Physical vapor deposition
- Chemical deposition
- Lithography
- Etching
- Back-end process
Ion implantation
Doping by ion implantation

- Several advantages compared to diffusion
- Ions are accelerated into a solid target for doping (e.g. for step 3)
- Both kinetic energy and dose can be accurately controlled
- Ultra thin junctions can be made
- Excellent doping uniformity across the wafer (< 1% variation across 12” wafer) and from wafer to wafer.
- Can be masked by thin films like photoresist or oxide
- Dopants are thermally activated after ion-implantation (substitutional position)

Typical parameters:

- Type of ion: P, As, Sb, B, O etc.
- Dose (D, # of atoms/cm²): $10^{11}$-$10^{18}$ cm⁻²
- Concentration (C, # of atoms/cm³), $D = \int_0^\infty C(x)dx$
- Ion flux ($\Phi$=D/t) $10^{12}$-$10^{14}$ cm⁻²s⁻¹, i.e. ~100nA-10 μA
- Acceleration energy: ~100ev- 1 MeV
Doping by ion implantation

9-10 different ion implantations during the full process!

Ion implanters

- Source/Channel/Drain
  - 50-200 nm deep
  - $10^{11}$-$10^{19}$ atoms/cm$^2$

- CMOS Well
  - 500-3000 nm deep
  - $10^{15}$-$10^{17}$ atoms/cm$^2$

Acceleration energy (keV)

Beam current (mA)
**Ion implanter**

- **Ion source**: ionization chamber operating at high voltage (25-60 kV) and converts the electrically neutral dopant atoms into plasma ions in the gas phase (Arsine, Phosphine, Diborane, BF₃) (p~1 mTorr). Ionizing electrons are emitted from the filament.

- **Mass separator**: a magnet bends the ion beam through right angle and selects the desired impurity ion and purge undesired species. Selected ion passes through an aperture \( \frac{1}{2}mv^2 = V_{ext}q \); \( qvB = M \frac{v^2}{R} \rightarrow \frac{M}{q} = \frac{R^2B^2}{2V_{ext}} \).

- **Accelerator**: adds energy to the beam up to 5MeV.

- **Scanning system**: x and y axis deflection plates to scan the beam across the wafer to produce uniform implantation of desired dose.
Doping by ion implantation

- Stopping power \( S \): retarding force acting on the charged particles due to interaction with matter, resulting in loss of particle energy
  \[
  S(E) = -\frac{dE}{dx}
  \]
  Projected range:
  \[
  R_P = \int_0^{E_0} \frac{1}{S(E)} dE
  \]

- At the beginning at high energies the ion is slowed down mainly by the electron cloud (electronic stopping, \( S_e \))
- When the ion has slowed down the collisions with nuclei become more and more probable (nuclear stopping, \( S_n \))
- When atoms of the solid receive significant recoil energies when struck by the ion, they will be removed from their lattice positions, and produce a cascade of further collisions in the material. These collision cascades are the main cause of damage production during ion implantation in metals and semiconductors.
Doping by ion implantation

- Gaussian distribution for first order approximation.
- \( R_p \): projected range (function of ion energy and mass, and atomic number of impurity as well as target material)
- \( \Delta R_p \): straggle (standard deviation)
- \( N_p = \) peak concentration at \( x = R_p \).
- Dose: \( \sqrt{2\pi N_p \Delta R_p} \)
Ion implantation + annealing

- Dopant has to be activated, that is bonded with four Si atoms (interstitial position)
- Annealing helps to recover damaged crystals
- Accompanied with the broadening of the profile which can be wanted or unwanted
2D/3D simulation of implantation profiles

- E.g. Monte Carlo simulation techniques (SRIM&TRIM, Athena/Silvaco)
- Design of the mask layer thickness
- Calculation of the p/n junction's location
- Design multiple implantation
- Simulate the effect of annealing
Silicon on Insulator (SOI) wafer by ion implantation

- Thin single crystal Si layer (device) on a buried oxide (BOX)
- To reduce parasitic device capacitance and leakage current
- Also often used for microelectromechanical systems (MEMS): membrane and cantilevers

Simox process
Patterning process
Patterning is one of the most critical operations in semiconductor processing. An IC wafer-fabrication process can require **40 or more** individual patterning steps.

**Goals of the operation**

- To **create**, in and on the wafer surface, a **pattern with the dimensions** established in the **design** phase of the IC.
- The **correct placement** of the circuit pattern on the wafer relative to the crystal orientation of the wafer and in a manner that all the layer parts are **aligned**.
Photolithography

- In microelectronics the most typical method to define a pattern is called **lithography**
- **Lithography** is traditionally a color printing method (λιθος - lithos: stone + γραφείν - graphein: to write) where a partially hydrophilic piece of stone or metal plate was immersed into ink and transferred to a substrate.

### Lithographic system

#### (a)
- Radiation source
- Illumination control system
- Resist coated sample

### Illumination process

- The resist is changed by the radiation

### Development

- The illuminated resist can be etched selectively to the unexposed resist
Classical 10-step photolithographic process

1. Surface preparation
   - Clean and dry wafer surface

2. Photoresist apply
   - Spin coat a thin layer of photoresist on surface

3. Soft bake
   - Partial evaporation of photoresist solvents by heating

4. Alignment and Exposure
   - Precise alignment of mask/reticle to wafer and exposure of photoresist. Negative resist is polymerized.

5. Development
   - Removal of unpolymerized resist

6. Hard bake
   - Additional evaporation of solvents

7. Develop inspect
   - Inspect surface for alignment and defects

8. Etch
   - Top layer of wafer is removed through opening in resist layer

9. Photoresist removal (strip)
   - Remove photoresist layer from wafer

10. Final inspection
    - Surface inspection for etch irregularities and other problems
Photolithography for etching

In **negative** resist: photopolymerization

In **positive** resist: photosolubilization
Photolithography for lift-off

- A simple technique for metal pattern
- Wet technique with high risk of failure → not applied in mass production
Lithographic classes

Contact

\[ \text{MFS} = \sqrt{d \cdot \lambda} \]

- Relatively low MFS
- Deterioration of the mask

Proximity

\[ \text{MFS} = \sqrt{(d + g) \cdot \lambda} \]

- Higher MFS because of the gap
- No mask deterioration

Projection

\[ \text{MFS} = k_1 \frac{\lambda}{NA} \]
\[ \text{DOF} = k_2 \frac{n \lambda}{NA^2} \]

- Highest resolution, dominant in high-end production
- Slower process, expensive instrumentation

**MFS:** Minimal Feature Size

- \(d\): thickness of the resist
- \(\lambda\): wavelength
- \(\text{NA} = \sin(\alpha) \cdot n\), numerical aperture
- \(\alpha\): half cone angle of illumination beam

**DOF:** depth of focus

- \(n\): refractive index of the medium between last optical element and substrate

**Constants:**

- \(k_1\): \(\sim 0.4\), 1st technology constant
- \(k_2\): 2nd technology constant
Typical contact photolithography tools

Spin-coater to cover the substrate with photoresist

Mask aligner to expose the photoresist through the mask

Developer to remove the exposed photoresist
Resolution enhancement: wavelength reduction

<table>
<thead>
<tr>
<th>Source</th>
<th>Range</th>
<th>$\lambda$ [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hg arc lamp</td>
<td>G-line, blue</td>
<td>436</td>
</tr>
<tr>
<td>Hg arc lamp</td>
<td>H-line, violet</td>
<td>405</td>
</tr>
<tr>
<td>Hg arc lamp</td>
<td>I-line, near UV</td>
<td>365</td>
</tr>
<tr>
<td>Hg/Xe arc lamp/KrF excimer laser</td>
<td>Deep UV (DUV)</td>
<td>248</td>
</tr>
<tr>
<td>ArF excimer laser</td>
<td>Deep UV (DUV)</td>
<td>193</td>
</tr>
<tr>
<td>Laser produced plasma; discharge produced plasma</td>
<td>Extreme UV (EUV)</td>
<td>13.5</td>
</tr>
<tr>
<td>X-ray tube, synchrotone</td>
<td>X-ray</td>
<td>~1</td>
</tr>
</tbody>
</table>

Spectrum of the Hg arc lamp

Vacuum UV (VUV): $\lambda=10-200$ nm; strong $O_2$ absorption $\lambda<200$ nm, while $N_2$ absorbs at $\lambda<150$ nm.
→ at deeper UV the instrumentation is getting more and more complicated and expensive.
Introducing an aperture will generate an effective light source which results in an off-axis illumination.

By an additional phase shifting layer on the mask the wavefront can be modified to utilize interference effect.

Blanking parts of the wave front after projection optics in pupil filtering also enhances the phase distribution on wafers.

Immersium medium, like DI water (n=1.44) helps to increase NA up to ~1.2.

With multiple exposures of the same structure the patterns are optimized.
Resolution enhancement by phase shifting technique

Modulation Transfer Function: \[ MTF = \frac{I_{\text{max}} - I_{\text{min}}}{I_{\text{max}} + I_{\text{min}}} \]

By an additional phase shifting layer we can benefit from the destructive interference.
Resolution enhancement by double patterning

Pitch split type double patterning

Sidewall spacer type double patterning
Extreme Ultraviolet (EUV) Lithography

- Not only the wavelength the price is also extreme!
- Used for the 7-nm technology since 2019
- Because of the strong absorption of matters there is no lens in this range
- Instead multilayer (Bragg) mirrors are used with a limited reflectance of ~70%
- After 12 reflections $I/I \sim 0.7^{12}=0.014$ (only about 1%!)
Thermal oxidation
Thermal oxidation: technology

- Converts Si on the wafer into SiO$_2$ to obtain high quality insulator e.g. for ion implantation masking
- Annealing at a T=800-1200 °C in a quartz or SiC tube furnace using a movable quartz rack (boat)
- Atmosphere:
  - Water vapor (wet): $\text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2(\text{g})$ (higher growth rate)
  - $\text{O}_2$ (dry): $\text{Si} + \text{O}_2 \rightarrow \text{SiO}_2$ (better quality)
- Growth occurs 54% above and 46% below the original surface as Si is consumed $X_{Si} = X_{ox} \frac{N_{ox}}{N_{Si}} = 0.46X_{ox}$
Thermal oxidation: growth kinetics

Gas Diffusion
Solid-state Diffusion
SiO₂ Formation

Oxidant Flow
(O₂ or H₂O)

Gas Flow
Stagnant Layer
SiO₂
Si-Substrate

Note
Cₛ ≠ C₀
Example:

A <100> silicon wafer has a 2000-Å oxide on its surface

(a) How long did it take to grow this oxide at 1100° C in dry oxygen?

(b) The wafer is put back in the furnace in wet oxygen at 1000° C. How long will it take to grow an additional 3000 Å of oxide?
Thin film deposition
CMOS materials

Film parameters

- Thickness/uniformity → well-controlled thickness over the wafer; trenches are challenging
- Surface flatness/roughness → can influence the subsequent layer
- Composition/grain size → stoichiometry is important; grain size will effect the electrical/mechanical properties
- Internal stress → have to be stress-free to avoid cracking accompanied often by contamination or short cut
- Purity → excluding mobile ions or oxygen from epitaxial layers
- Electrical properties → metals with high conductivity, low-k dielectrics, high-k dielectrics etc

Non-uniformity in deep trenches; aspect ratio (depth/width) plays an important role
**Film deposition methods: categories**

- In CVD, the wafer is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposit.
- PVD is a process in which the material goes from a condensed phase to a vapor phase and then back to a thin film condensed phase.

<table>
<thead>
<tr>
<th>Production mechanism of depositing species</th>
<th>Chemical Vapor Deposition (CVD)</th>
<th>Physical Vapor Deposition (PVD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deposition rate</td>
<td>Low, moderate</td>
<td>High, up to 75 nm/min</td>
</tr>
<tr>
<td>Deposition Species</td>
<td>Precursor molecules</td>
<td>Atoms and ions</td>
</tr>
<tr>
<td>Energy of deposited species</td>
<td>Low, can be high with plasma-aid</td>
<td>Low, 0.1-0.5 eV</td>
</tr>
<tr>
<td>Scalable to wafer size</td>
<td>Up to large</td>
<td>Up to large</td>
</tr>
</tbody>
</table>

- **Chemical Vapor Deposition (CVD)**
  - LPCVD, MOCVD etc.
  - Production mechanism of depositing species: Chemical reaction
  - Deposition rate: Low, moderate
  - Deposition Species: Precursor molecules
  - Energy of deposited species: Low, can be high with plasma-aid
  - Scalable to wafer size: Up to large

- **Physical Vapor Deposition (PVD)**
  - Production mechanism of depositing species: Thermal energy
  - Deposition rate: High, up to 75 nm/min
  - Deposition Species: Atoms and ions
  - Energy of deposited species: Low, 0.1-0.5 eV
  - Scalable to wafer size: Up to large

- **Pulsed Laser Deposition (PLD)**
  - Production mechanism of depositing species: Momentum transfer
  - Deposition rate: Low, moderate
  - Deposition Species: Atoms and ions
  - Energy of deposited species: Can be high, 1-100 eV
  - Scalable to wafer size: Limited
Film deposition methods: gas kinetics

Using Maxwell velocity distribution:

\[
\lambda = \frac{1}{\sqrt{2\pi N d^2}} = \frac{k_B T}{\sqrt{2\pi p d^2}}
\]
Chemical vapor deposition (CVD)

- Wafer is exposed to one or more volatile precursor which react and/or decompose on the substrate surface to produce high quality thin film
- Volatile by-products are removed by gas flow through the reaction chamber
- Materials in various forms: epitaxial, polycrystalline, amorphous
- Materials: Si, SiO$_2$, SiC, Si$_x$N, SiON, W, high-k dielectrics, low-k dielectrics
- High quality, conformal deposition (high step coverage)
- For example:
  
  poli Si at 580-650 °C and ~1 mbar: \[ \text{SiH}_4 \leftrightarrow \text{Si(s)} + 2\text{H}_2 \]
  
  Si$_3$N$_4$ at 700-900 °C and atm. Pr.: \[ 3\text{SiH}_4 + 4\text{NH}_3 \leftrightarrow \text{Si}_3\text{N}_4(s) + 12\text{H}_2 \]
Chemical vapor deposition (CVD)

Several subcategories and reactor designs:

- By operation conditions: atmospheric, low-pressure (LPCVD), ultrahigh vacuum
- Plasma methods: plasma-enhanced (PECVD), remote plasma enhanced (RPCVD)
- By the precursor: e.g. metalorganic chemical vapor deposition (MOCVD)
Atomic Layer Deposition (ALD)

- A subclass of chemical vapor deposition based on subsequential use of gas phase chemical process
- Two precursors react with the surface of the material one at a time in a sequential, self-limiting manner
- Atomic control of the layers, but slow growing rate
- Both metals and (high-k) dielectrics; key method in the fabrication of semiconductor devices
- Main setting parameters: substrate temperature, pulse times for precursors and purging, temperature of the precursor container
- Plasma assisted mode is also possible
Evaporation type PVD

• Heating of a solid material inside a high vacuum chamber, taking it to a temperature which produces some vapor pressure (often melting)
• Since \( E_{\text{kin}} < 1 \text{ eV} \rightarrow \) High vacuum is needed \((< 10^{-4} \text{ Torr})\) for \( \lambda > D_{\text{source-substrate}} \)
• Directional material transfer: vapor stream traversing the chamber and hitting the substrate (for uniform layer: planetary movement of the wafers, for lift-off process: fix sample position)
• Heating of the source: resistive and e-beam evaporation
• In thermal evaporation: resistively heating element \((\sim 50-100 \text{ A, } \sim 6-20 \text{ V})\) made of a refractory material (boat or filament)
• Most system use Quartz Crystal Microbalance for real-time monitoring of deposition rate \((S \sim \mu g/cm^2)\)
E-beam evaporator uses an electron beam to heat up source material to vapor phase
- E-beam is magnetically directed (270°) into the crucible of the source material
- Very high power density: ~ 10 kV, ~ 0.1 A, ~ 1 kW absorbed in a small volume
- Water cooled container
- Programmed e-beam scanning for the uniform usage of the source
- Several material can be deposited using multiple crucible
- More developed than thermal evaporation. Benefits:
  - Less contamination from the crucible material
  - Very high deposition rate
  - High material utilization efficiency
PVD2: Sputtering

- A kind of physical vapor deposition (PVD) process for thin films
- Particles are ejected from the solid target due to ion bombardment
- Due to higher kinetic energy, better adhesion to the substrate than in case of vacuum evaporation
- Done either using DC voltage (DC sputtering) or AC voltage (13,56 MHz, RF sputtering)
- Metals can be deposited by DC or pulsed DC
- Insulators can be deposited either from ceramic target by RF or from metallic target in reactive atmosphere (e.g. AlN from Al in N₂ atmosphere)
- Can be combined with e-beam evaporators
Combined PVD-CVD cluster systems

- Automatic deposition of subsequent layers without breaking the vacuum during the process
Etching process
Etching techniques

**Wet etching**
- Liquid etchant
- Chemical reaction
- High selectivity

**Dry etching**
- Vapor phase etchants
- Chemical and physical processes
- Lower selectivity

**Isotropic**
E.g. HF-HNO$_3$-CH$_3$COOH (polishing etchant): etching rate is not direction dependent

**Anisotropic**
E.g. KOH etch: Etching rate depends on the crystal faces
Dry etching

- More efficient **chemical** etching using reactive radicals (e.g. atomic F) (Plasma etching)
  - $\text{CF}_4 + e^- \rightarrow \text{CF}_3 + \text{F} + e^-$
  - $4\text{F} + \text{Si} \rightarrow \text{SiF}_4$
- More anisotropic **physical** etching by charged particles (Ion milling)

operations are often combined:
Reactive Ion Etching (RIE)

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Reactive vs. physical ion etching

![Reactive vs. Physical Ion Etching Diagrams](image-url)

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Planar plasma etcher

![Planar Plasma Etcher Diagram](image-url)
Interconnection metalization
Back-end of the line (BEOL) interconnections

- Traditional IC connectors are made of Al
- Lower resistivity is needed to improve the performance (lower Joule heating, higher current density)
- Challenge with Cu patterning; doesn’t produce volatile byproduct
- Solution: **Damascene process** (introduced by IBM in the 1990s)

**Damascene gold plate**
Damascene process

Instead of etching the metal via photolithography pattern, gaps in low-k dielectric are filled by PVD seed layer and electroplated Cu.

Chemical mechanical polishing

State-of-the-art SRAM

Fig. 2: Single Damascene Process Steps [1]
Video