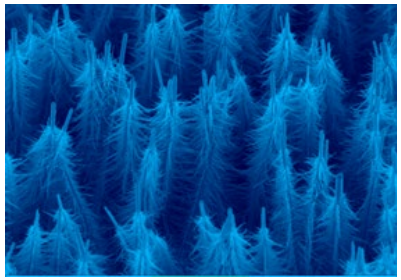
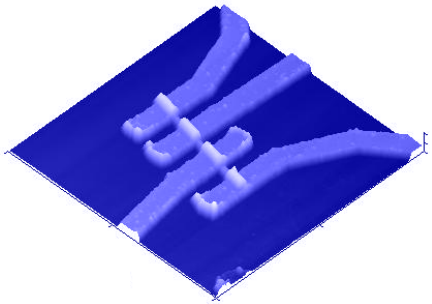
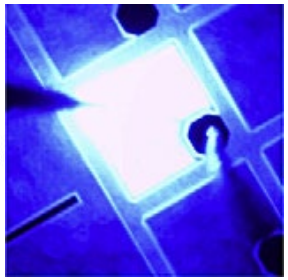
Semiconductor Physics

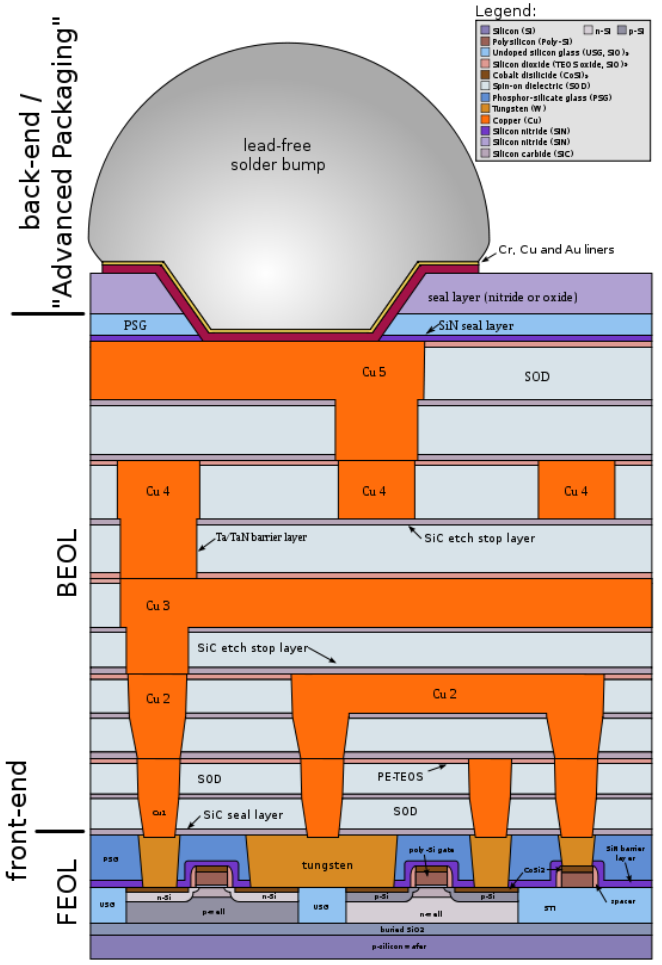
János Volk

BME TTK, Nov. 27th, 2018
volk@mfa.kfki.hu

Outlook

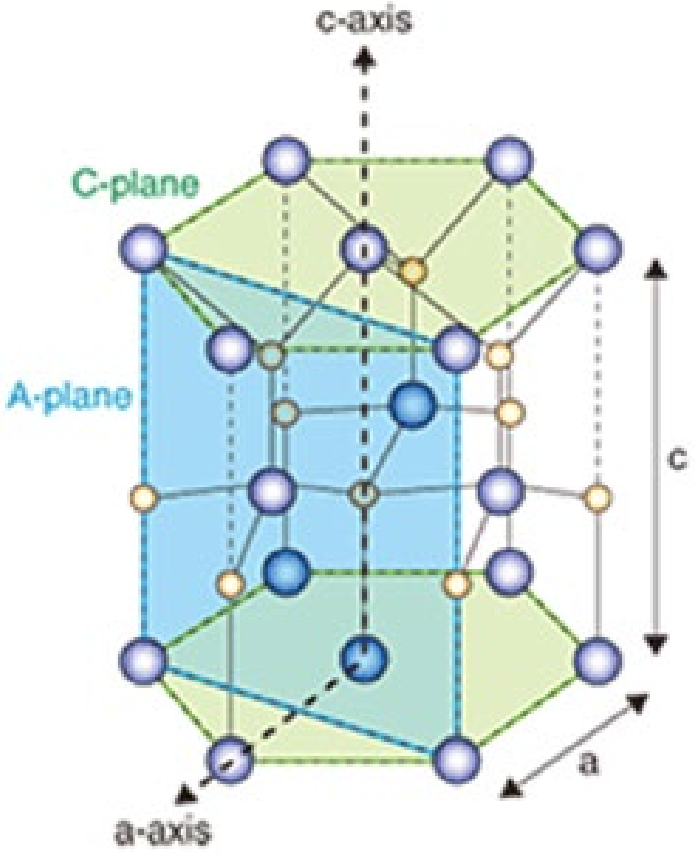
- GaN HEMT
  - Polar semiconductors
  - 2DEG and HEMT
- Si technology
  - Si crystal
  - Thin film formation
  - Etching techniques
  - Lithography
  - Ion implantation
- Trends
  - Future CMOS
  - More than more

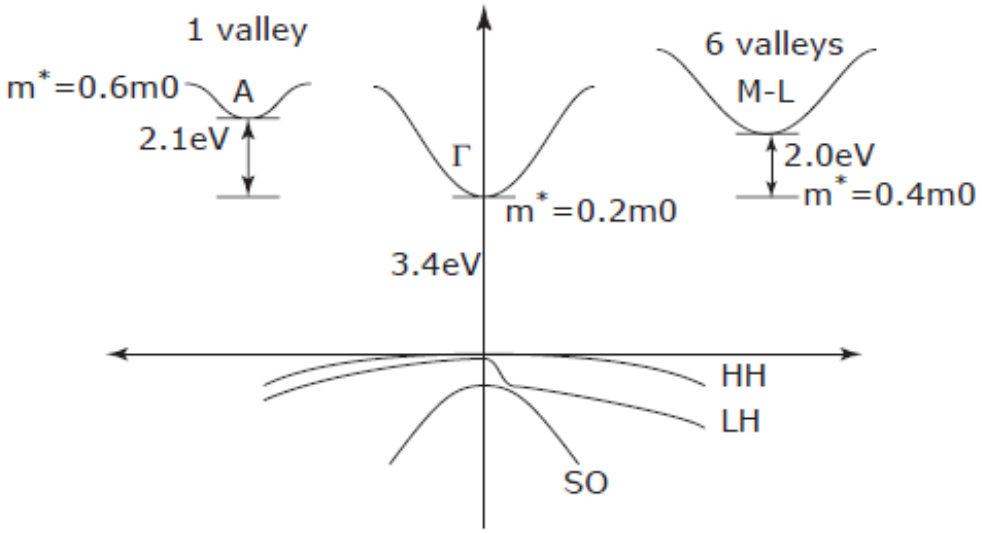


GaN HEMT

Polar semiconductors

- Lack of crystal inversion symmetry
- Relatively low band gap, i.e. not insulator
- E.g. semiconductors in wurtzite crystal group (GaN, ZnO, AlN, SiC, CdS stb.)

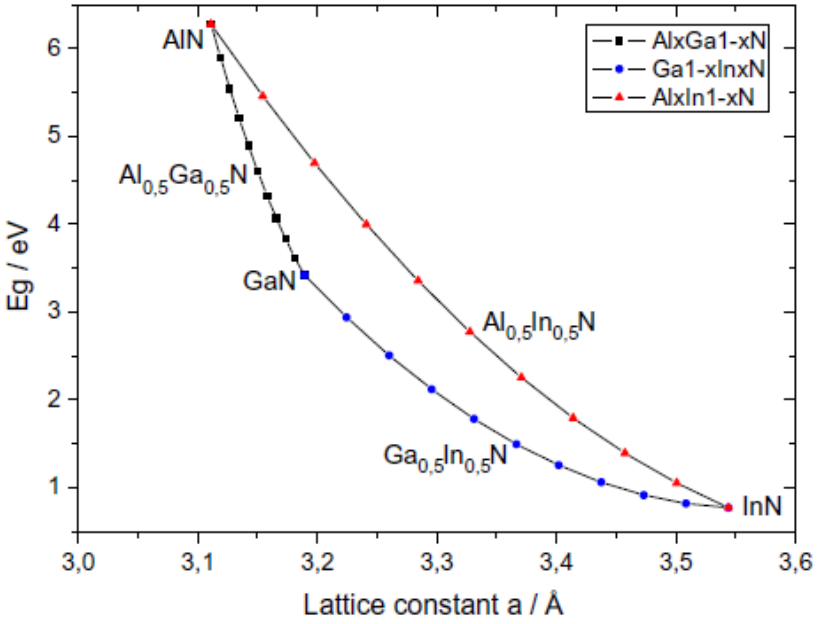




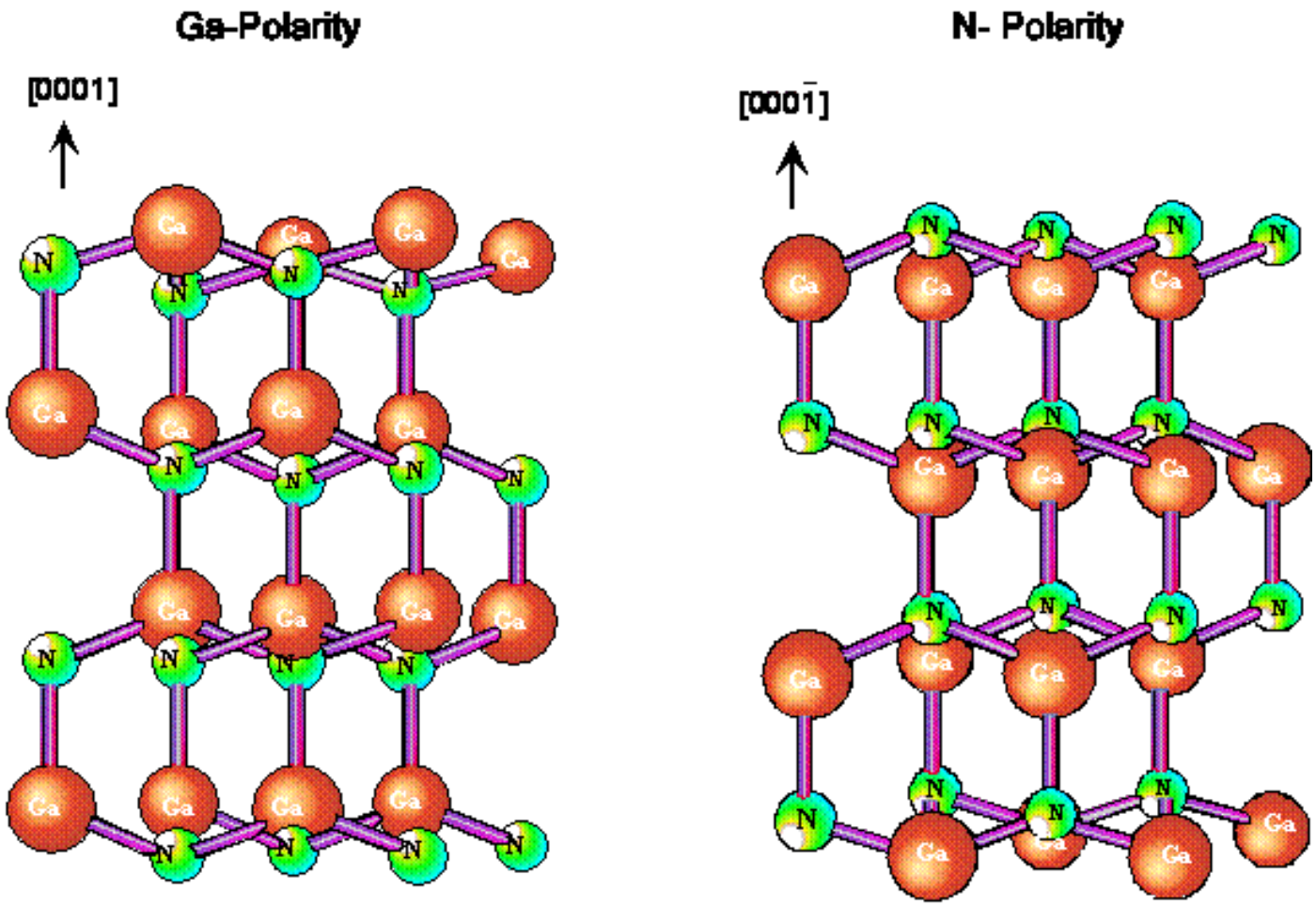
Simplified band structure of GaN

Merits of GaN

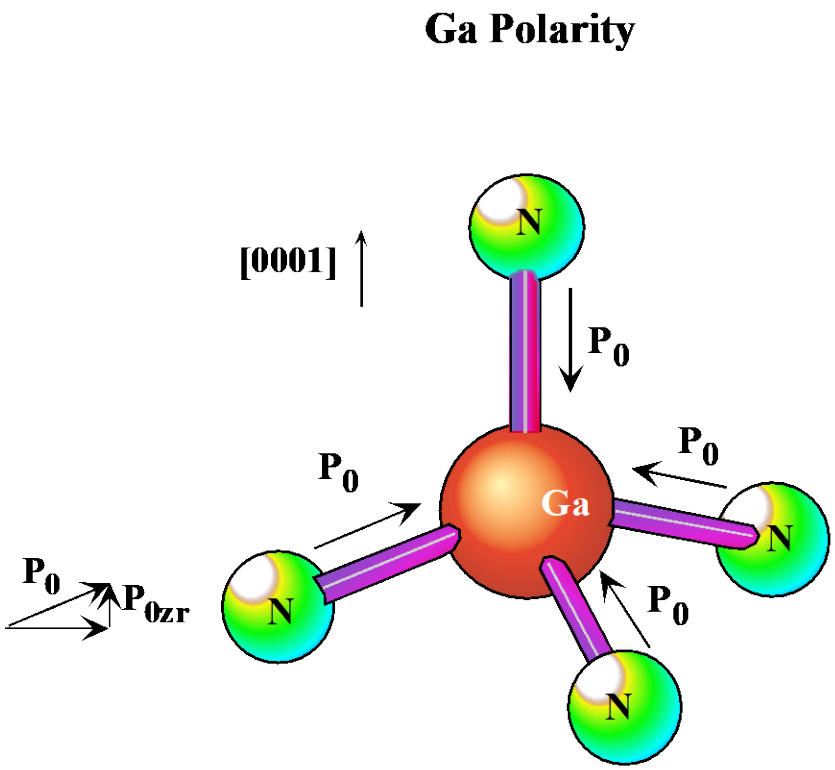
- Epi-ready substrates are available: sapphire, SiC, Si (8”), AlN, GaN
- Band-gap engineering: AlGaN, InGaN
- Deposition methods:
  - MOCVD (MOVPE) (industrial)
  - MBE (research)

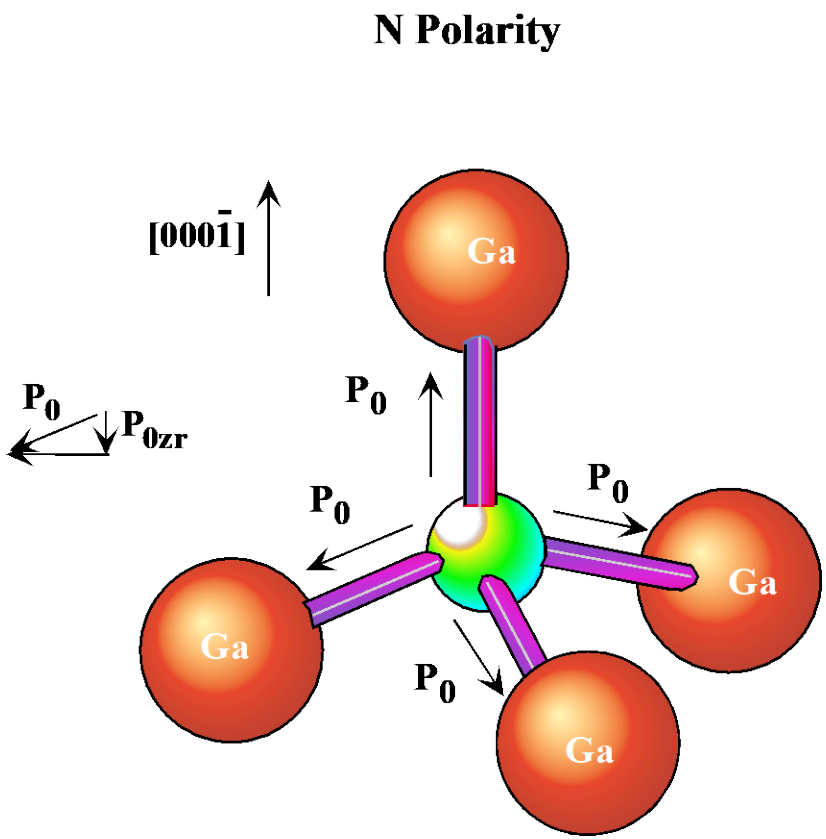


Crystal polarity

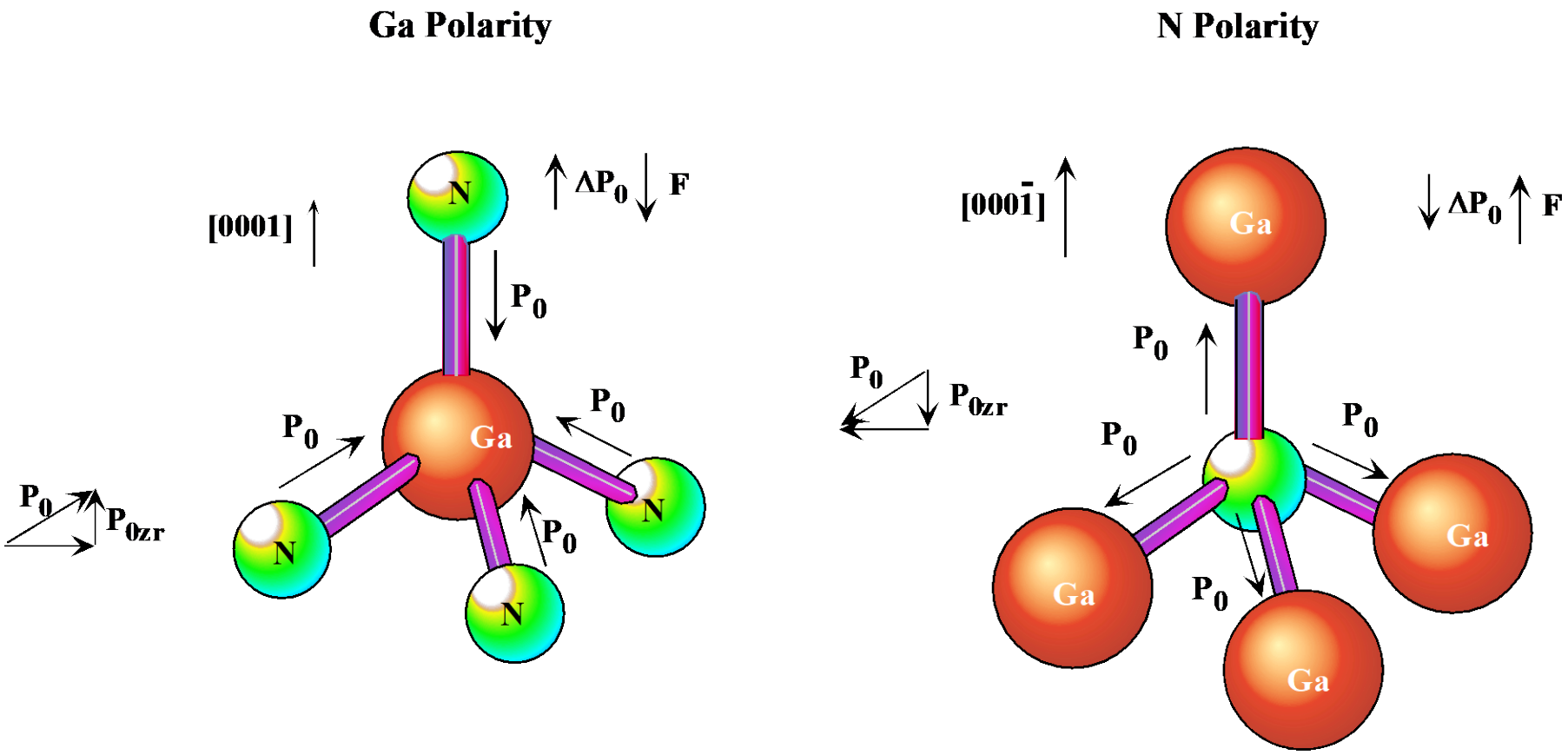


Wurtzite crystal: relaxed

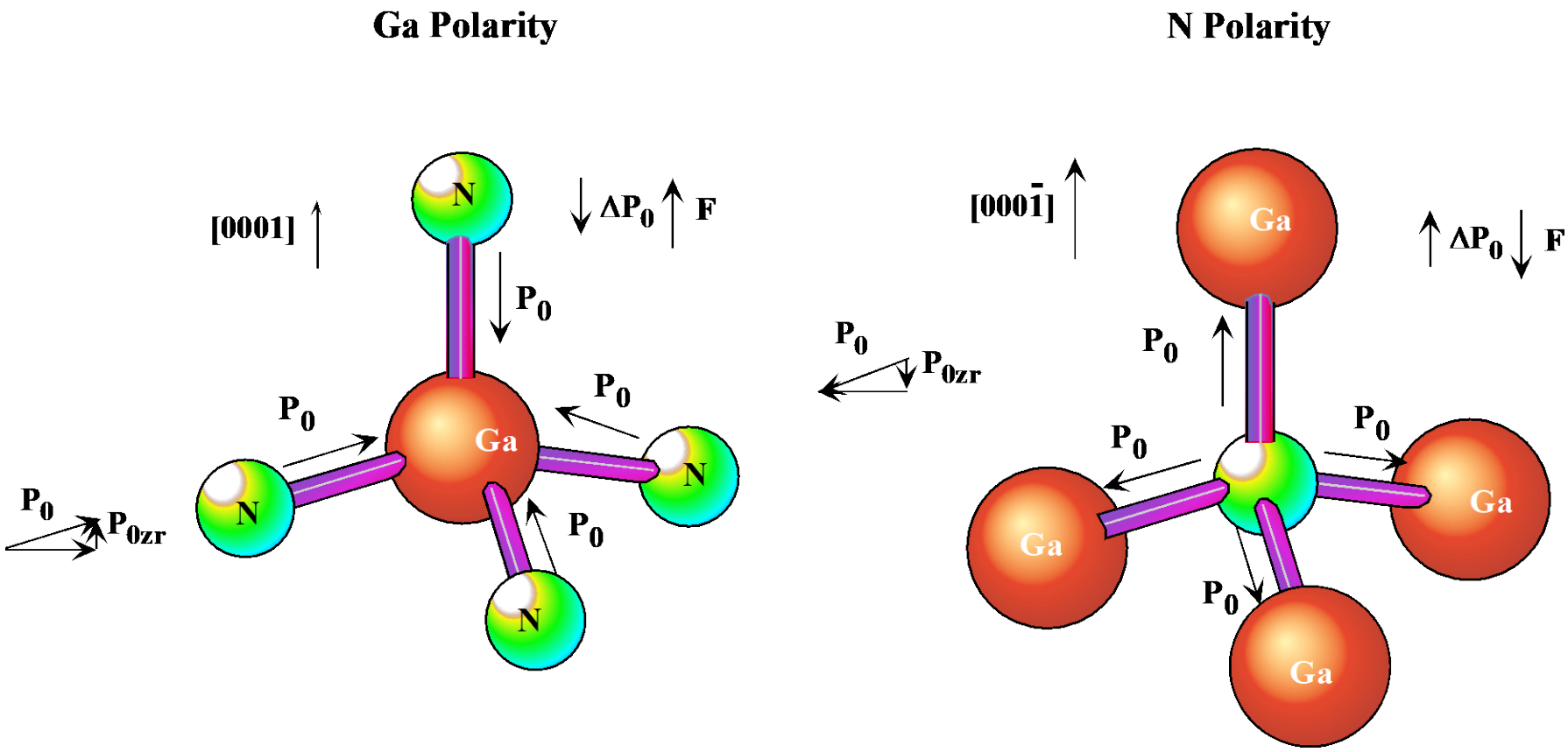




Wurtzite crystal: tensile stress



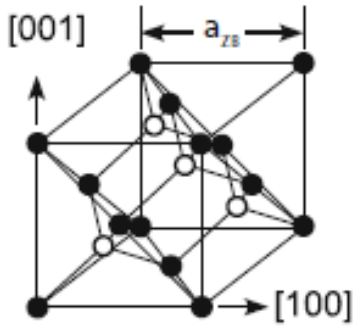
Wurtzite crystal: compressing stress



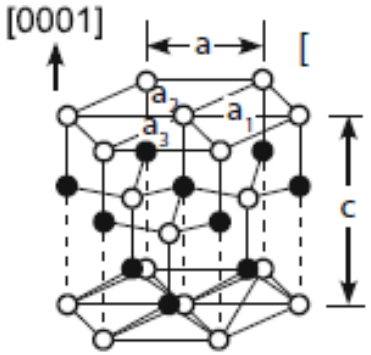
Piezoelectric polarization

- It plays an important for pseudomorphic epiatxial layers

Spontaneous polarization in wurtzite crystal



fcc (abcabc…)



Wurtzite (hcp: abab..)

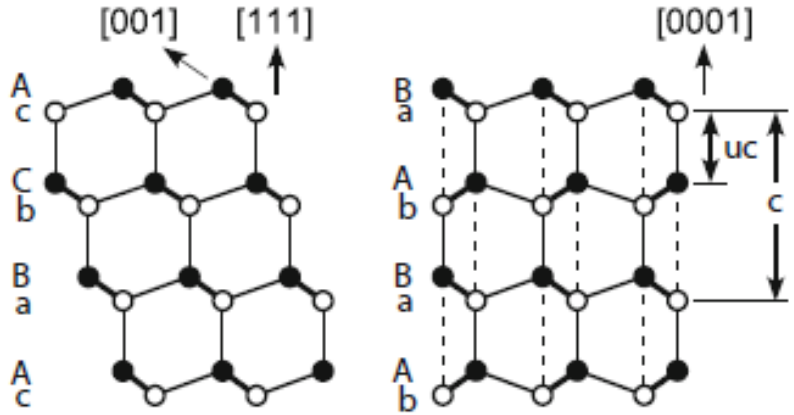
$$\left(\frac{c}{a}\right)_{hcp} = \sqrt{\frac{8}{3}} = 1{,}633$$

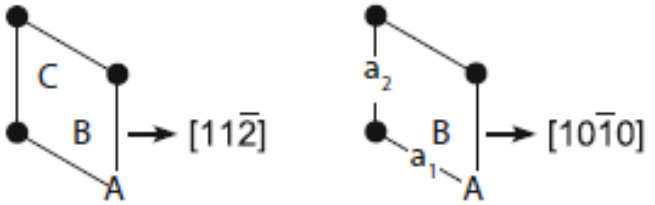
Ideal value from atomic ball model

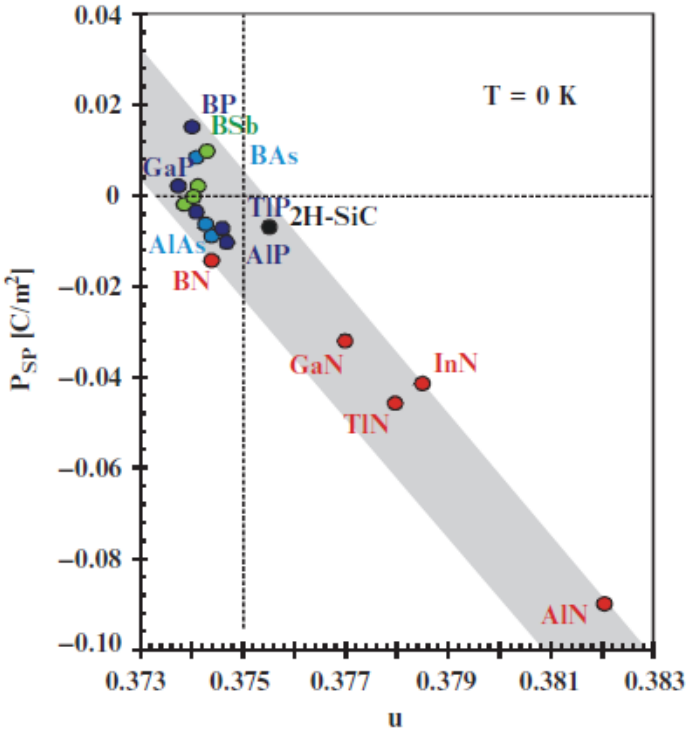
$$u_{hcp} = \frac{3}{8} = 0{,}375$$

$$ha\ u \neq u_{hcp}$$

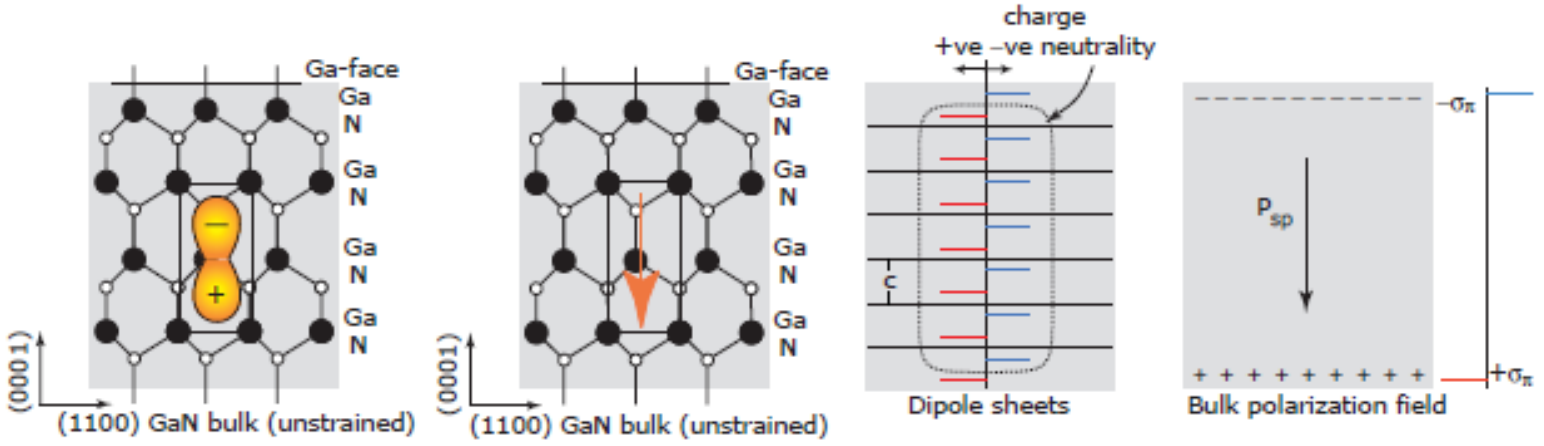
Spontaneous polarization







Spontaneous polarization



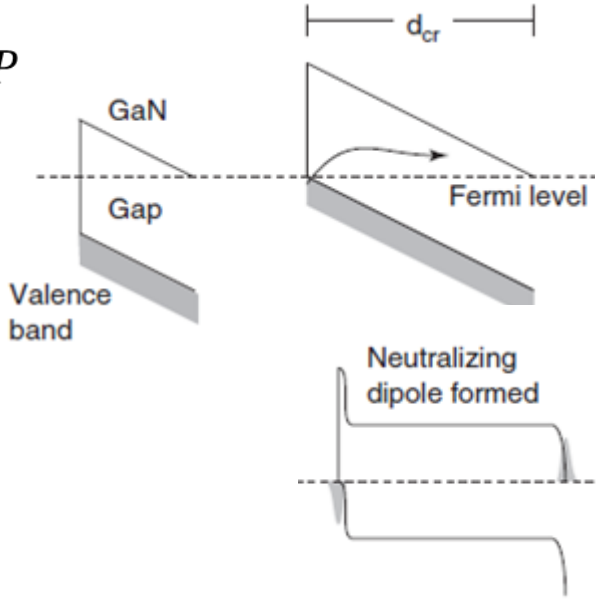
Polarization induced charges: $\rho_P = -\nabla P$

Field~ 1-10 MV/cm

In metals: screening of free carriers

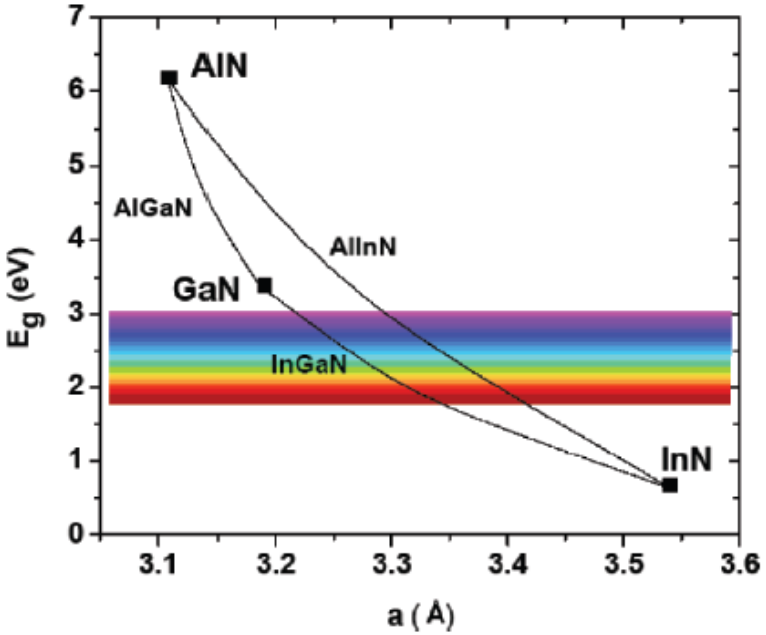
Insulators: unscreened fix charges

Semiconductors: screening above the critical value

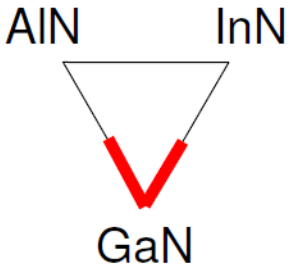


Most important case on epitaxial single crystals!

Epitaxial growth and lattice mismatch

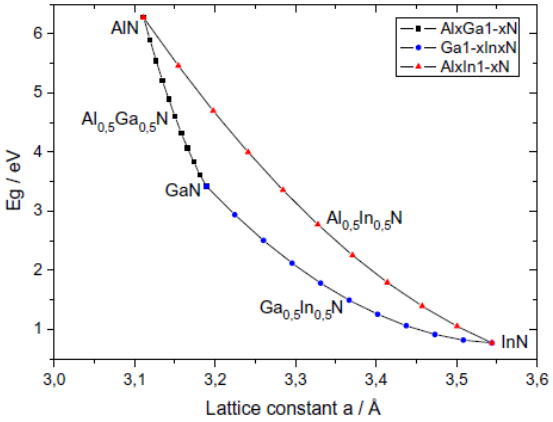


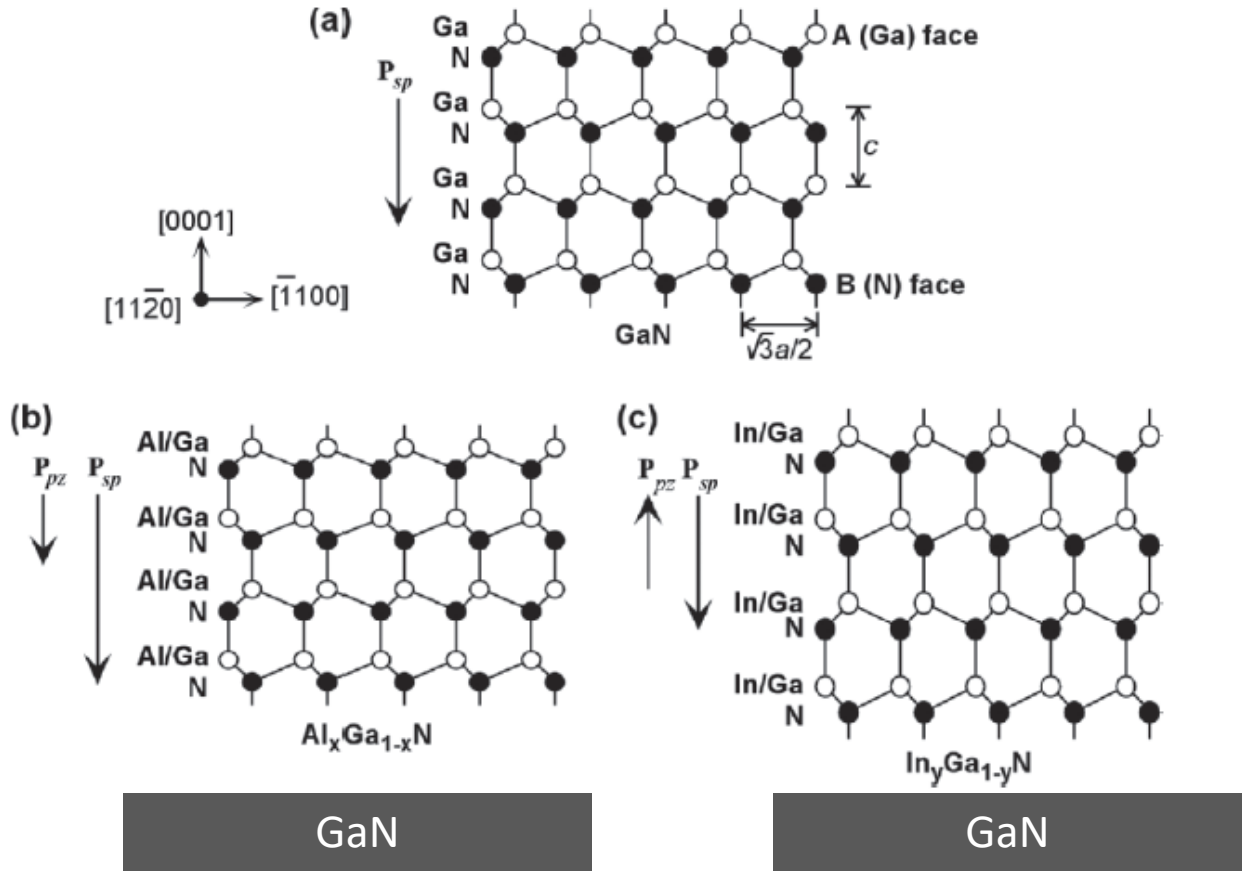
Material	AlN	GaN	InN
c_0/a_0[a]	1.6010	1.6259	1.6116
P_{SP}(C/m^2)[a]	−0.081	−0.029	−0.032



- The bandgap and lattice parameters can be tuned in wide by changing the composition ($Al_xGa_{1-x}N$, $In_xGa_{1-x}N$, $Al_xIn_{1-x}N$).
- The physical parameters of the alloy can be estimated by Vegard's law (simple interpolation).
- High quality heterojunctions can be deposited using metal organic chemical vapor deposition.

Polarization on heterojunctions

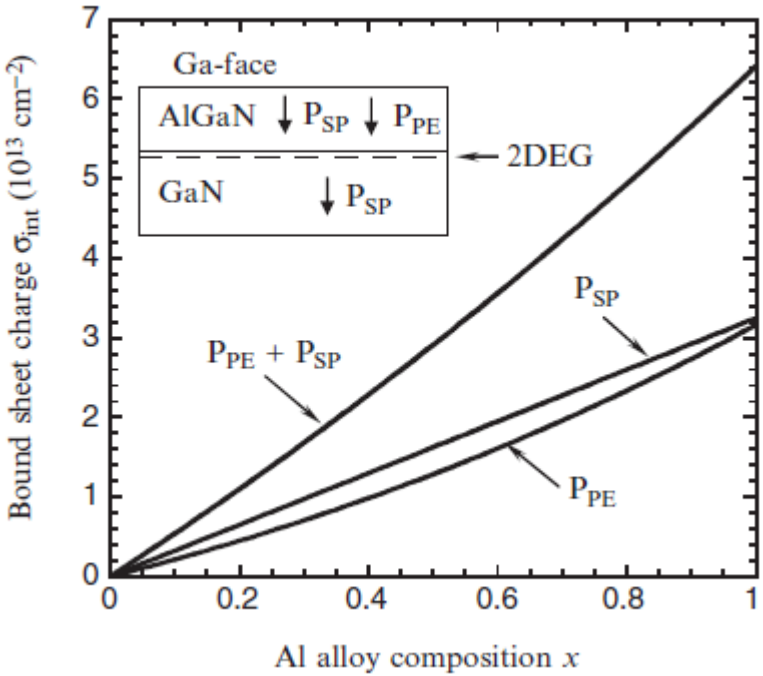


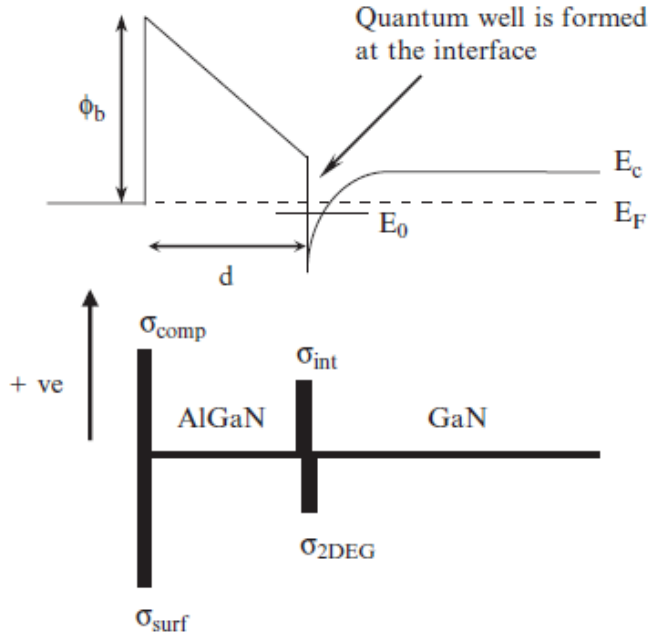


Piezoelectric polarization in case of biaxial stress:

$$P_z = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right),$$

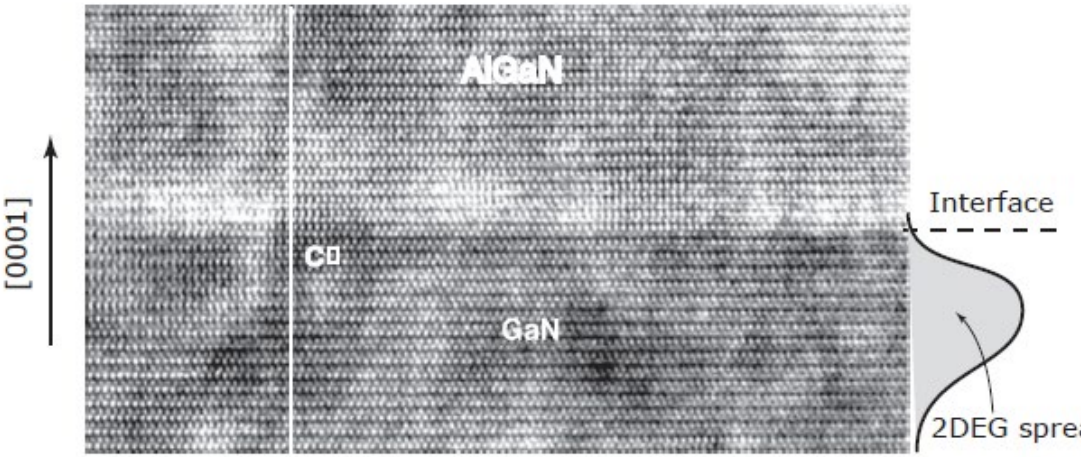
Two-dimentional electron gas (2DEG) at the heterointerface



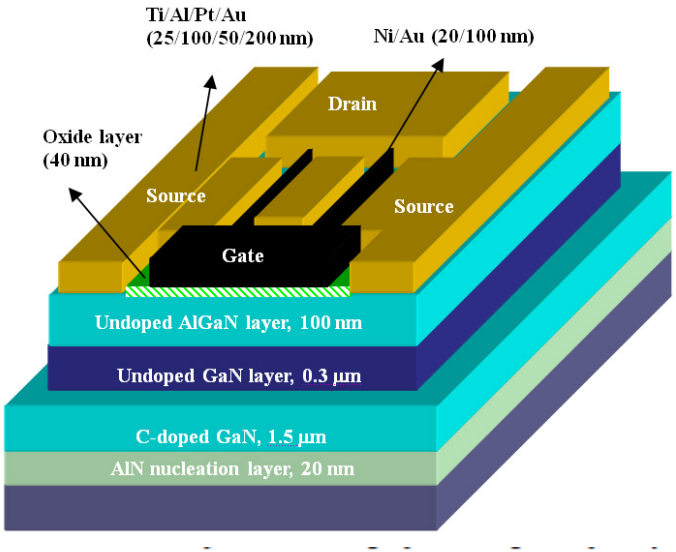


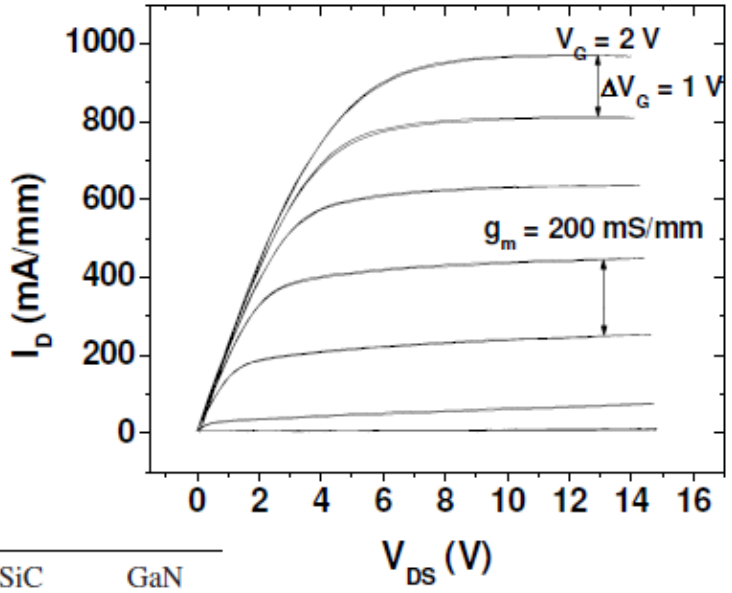
2DEG density:

$$n_s = \frac{+\sigma_B}{e} - \left(\frac{\varepsilon\varepsilon_0}{de^2}\right)\left[\Phi_B + E_F(n_s) - \Delta E_c\right]$$



Application: high electron mobility transistor





	Si	GaAs	Diamond	SiC	GaN
μ (cm^2/Vs)	600	8500	2200	1000	1600
Eg (eV)	1.12	1.43	5.45	3.26	3.40
v_{sat} (10^7 cm/s)	1.0	1.0	2.7	2.0	2.0
E_{break} (kV/cm)	300	400	10,000	2,200	2,000
Thermal conductivity (W/cmk)	1.5	0.46	22.0	4.40	2.30

Advantage: No impurity scattering since the channel is pure GaN. (At room temperature optical phonon scattering dominates.)

➡ High frequency devices and high power devices (U_{br}~200V, P~30 W/mm)

Si CMOS technology

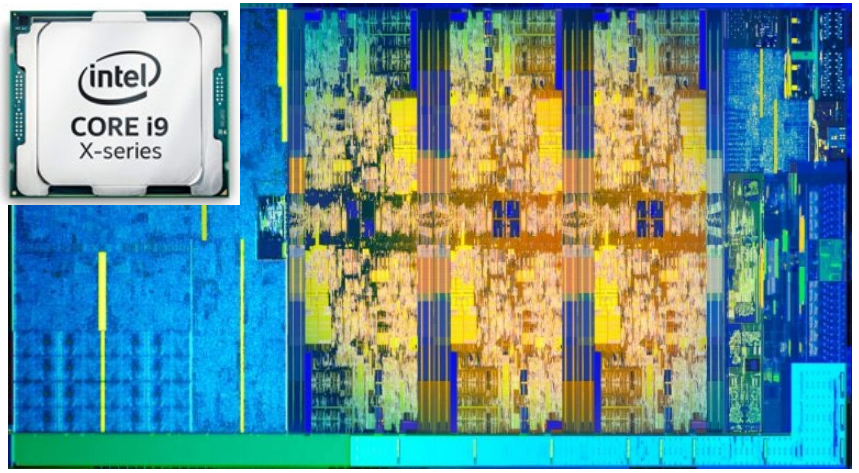
IC industry: Success story of the last 70 years

Discrete device

Point contact **Trans**fer res**istor** (1947)
J. Bardeen, W. Brattain, W. Shockley
(Nobel price in 1956)

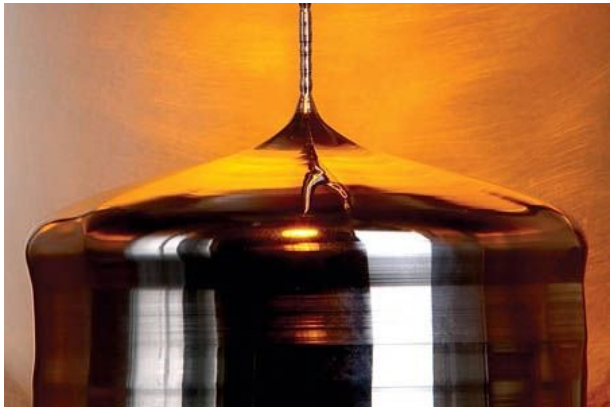
Ultra-large-scale integration (ULSI)

3 billion transistors on single chip
fabricated by 14-nm node technology

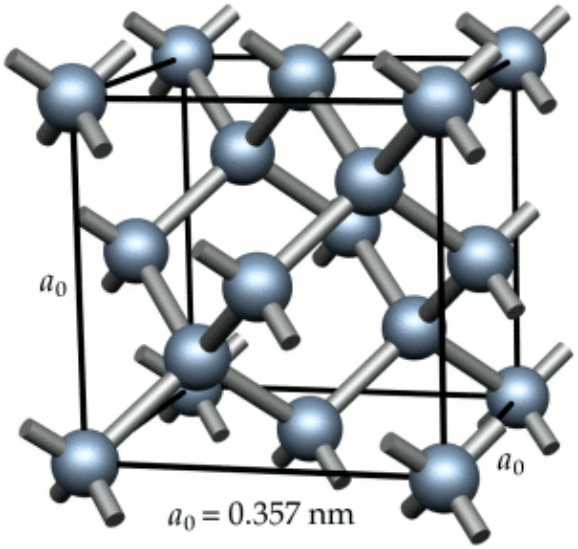


Si single crystal

High quality single crystal in large size



Single crystal Si grown by Czochralski method



Face central cubic crystal (fcc)

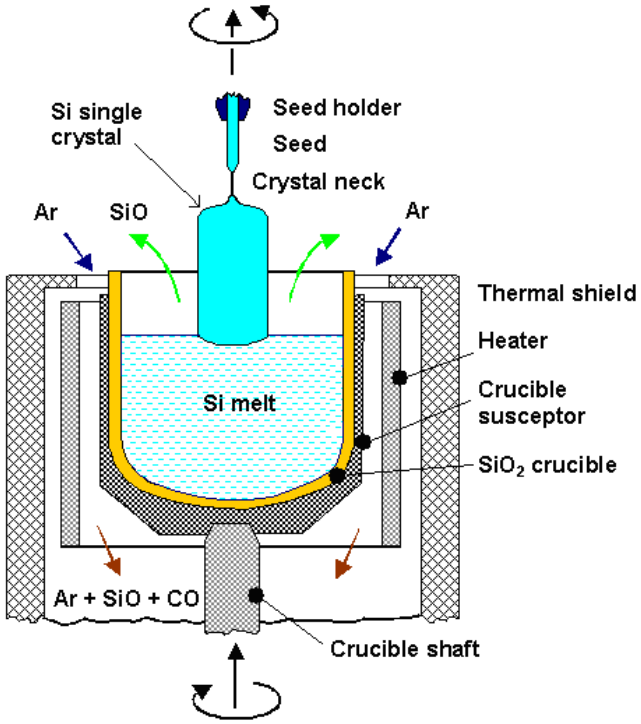
+ advantageous physical properties and good quality native oxide

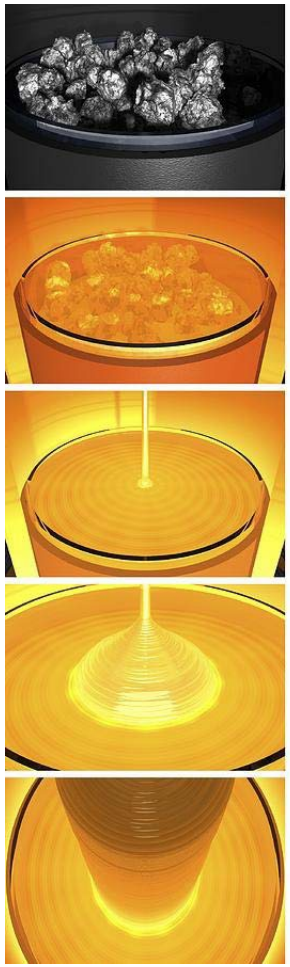
- Microelectronics is based on mainly on **Si**.
- III-V semiconductors play an important role in optoelectronics.

Czochralski method

- Polysilicon nuggets with the dopants are melted in the quartz crucible at a T>1400°C
- Purity of the polysilicon nuggets 99.9999999% (9N)

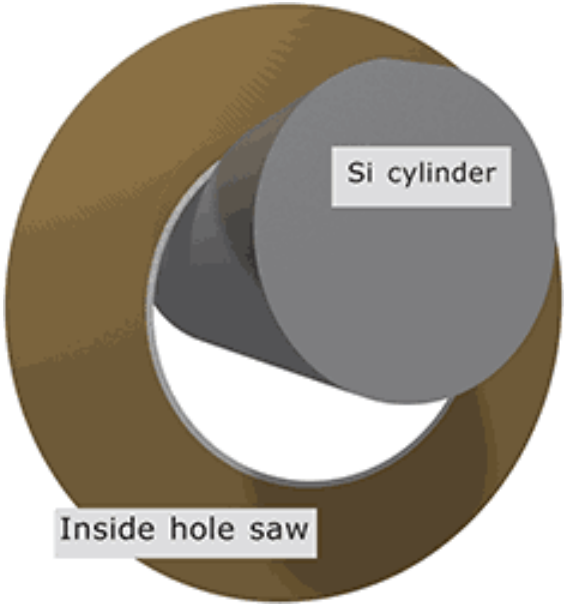
- Si crystal Si crystal with the desired orientation (<100>, <110> , <111> is slowly pulled out; both the seed and the crucible is rotated to maintain homogeneity
- Typical impurity concentration: N_O: 10^{18} cm^{-3}, N_C: 10^{17} cm^{-3} (N_{Si}=$5 \cdot 10^{22}$ $1/cm^3$)





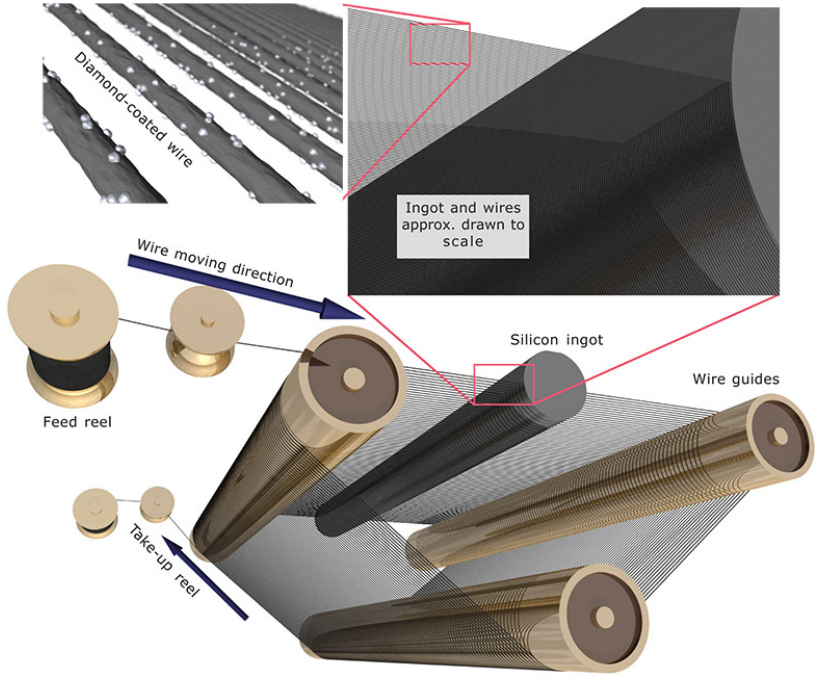
Wafer processing

Annular saw



- Wafer surface is relatively smooth, subsequent steps takes less time
- Low throughput

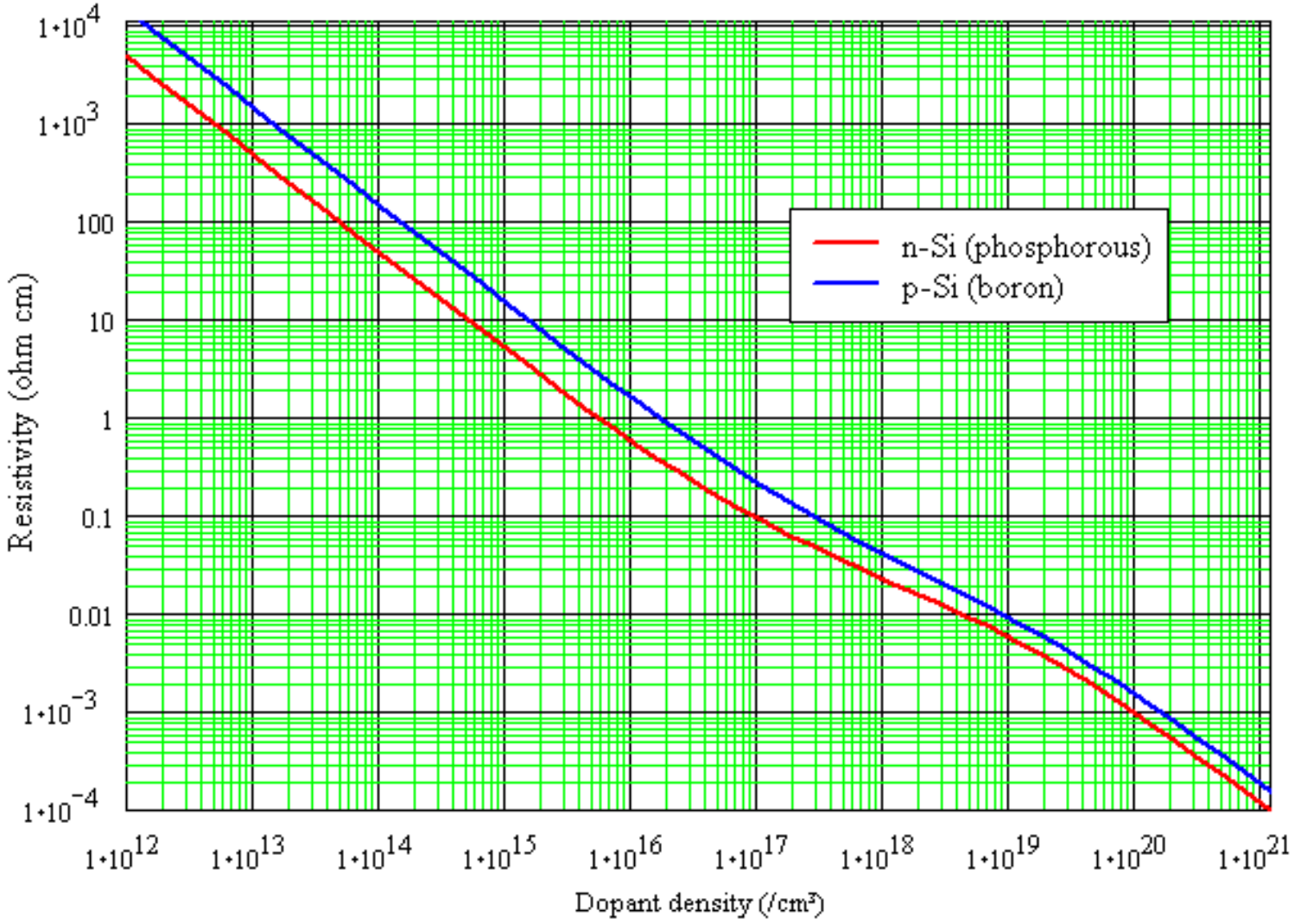
Wire saw



- Wafer surface is relatively smooth, subsequent lapping takes less time
- Low throughput

The process is continued and finished by lapping, etching, polishing and cleaning

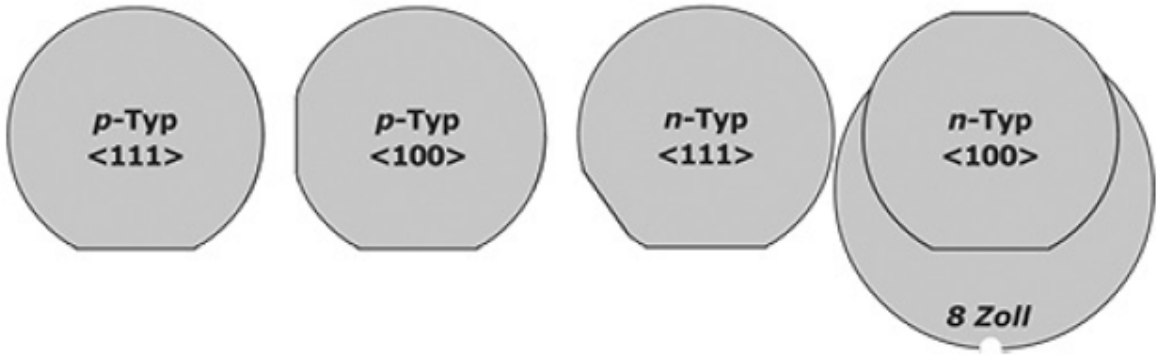
Wafer doping



Si wafer specification

Diameter (mm)	Growth	Dopant	Orientation	Finish	Coating
☐ 50.8	☐ CZ	☐ B	☐ <100>	☐ Single Side	☐ With
☐ 76.2	☐ FZ	☐ Ph	☐ <111>	☐ Double Side	☐ Without
☐ 100		☐ Sb	☐ <110>	☐ As Cut	
☐ 125		☐ As		☐ As Lapped	
☐ 150		☐ Undoped		☐ Ground	
☐ 200		☐ Intrinsic		☐ Etched	
☐ 300					

TTV	Bow	Warp	Thickness	Resistivity
≤	≤	≤	min ≥	min ≥
			max ≤	max ≤



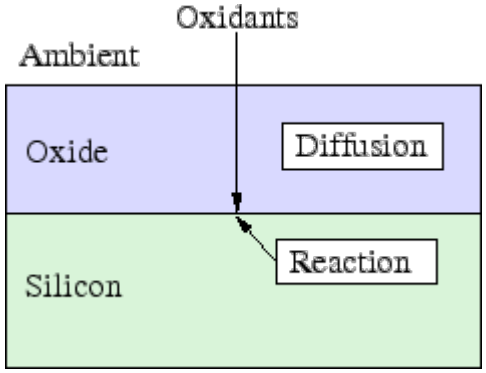

12” Si wafer (300 mm)

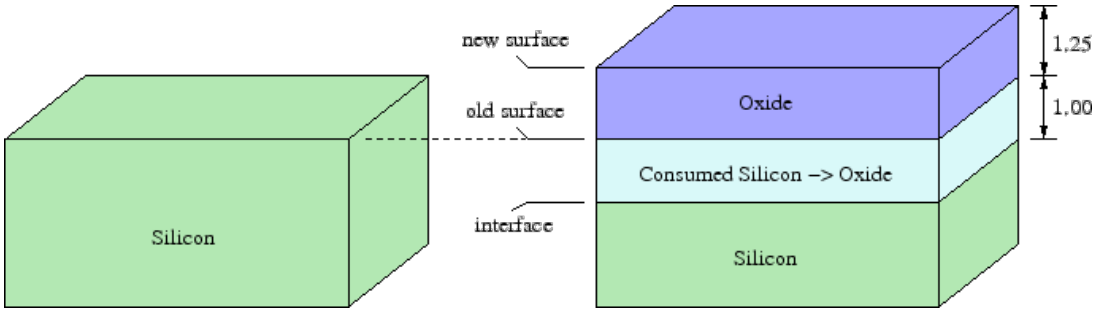
Thin film formation

- Thermal oxidation
- Physical Vapor Deposition (PVD)
- Chemical Vapor Deposition (CVD)
- Electroplating

Thermal oxidation

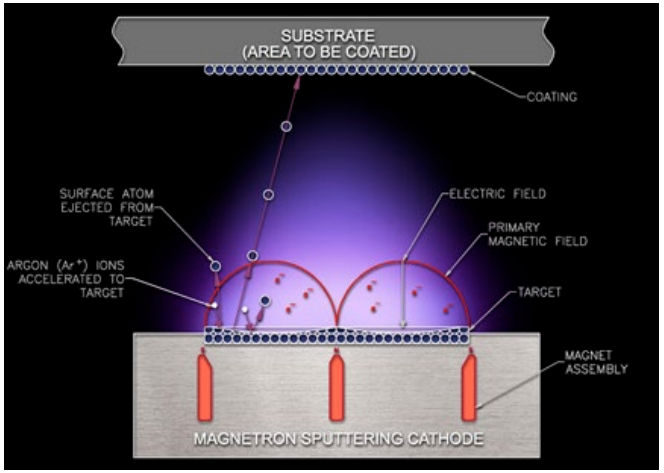
- Converts Si on the wafer into SiO_2 to obtain high quality insulator or mask for ion implantation
- Annealing at a T=800-1200 °C in a quartz or SiC tube furnace using a movable quartz rack (boat)
- Atmosphere:
  - Water vapor (wet): $Si+2H_2O \rightarrow SiO_2+2H_{2\ (g)}$ (higher growth rate)
  - O_2 (dry): $Si+O_2 \rightarrow SiO_2$ (better quality)
- Domination of Si in the IC industry is partly due to the high quality thermal oxide

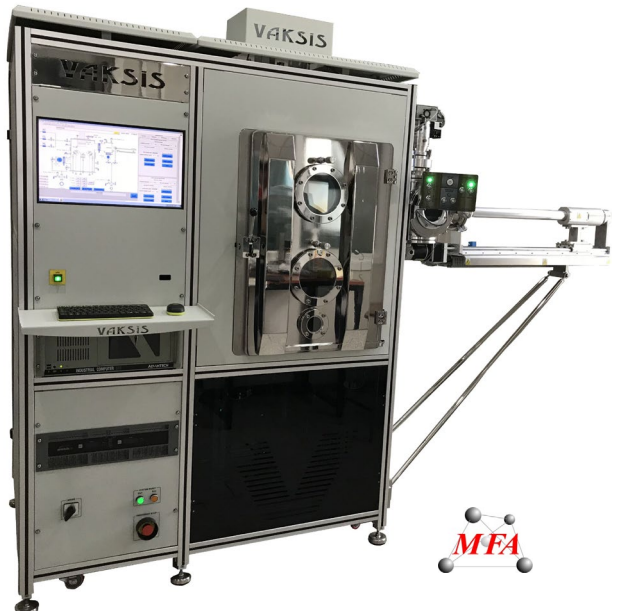




Sputter deposition (sputtering)

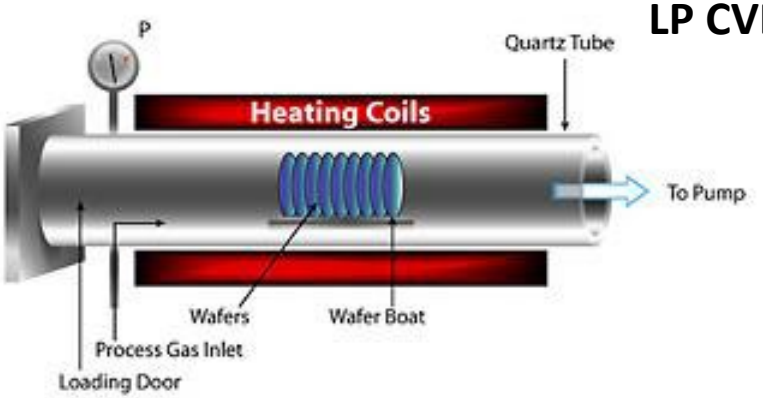
- A kind of physical vapor deposition (PVD) process for thin films
- Particles are ejected from the solid target due to ion bombardment
- Due to higher kinetic energy, better adhesion to the substrate than in case of vacuum evaporation
- Done either using DC voltage (DC sputtering) or AC voltage (13,56 MHz, RF sputtering)
- Metals can be deposited by DC or pulsed DC
- Insulators can be deposited either from ceramic target by RF or from metallic target in reactive atmosphere (e.g. AlN from Al in N_2 atmosphere)





Chemical vapor deposition (CVD)

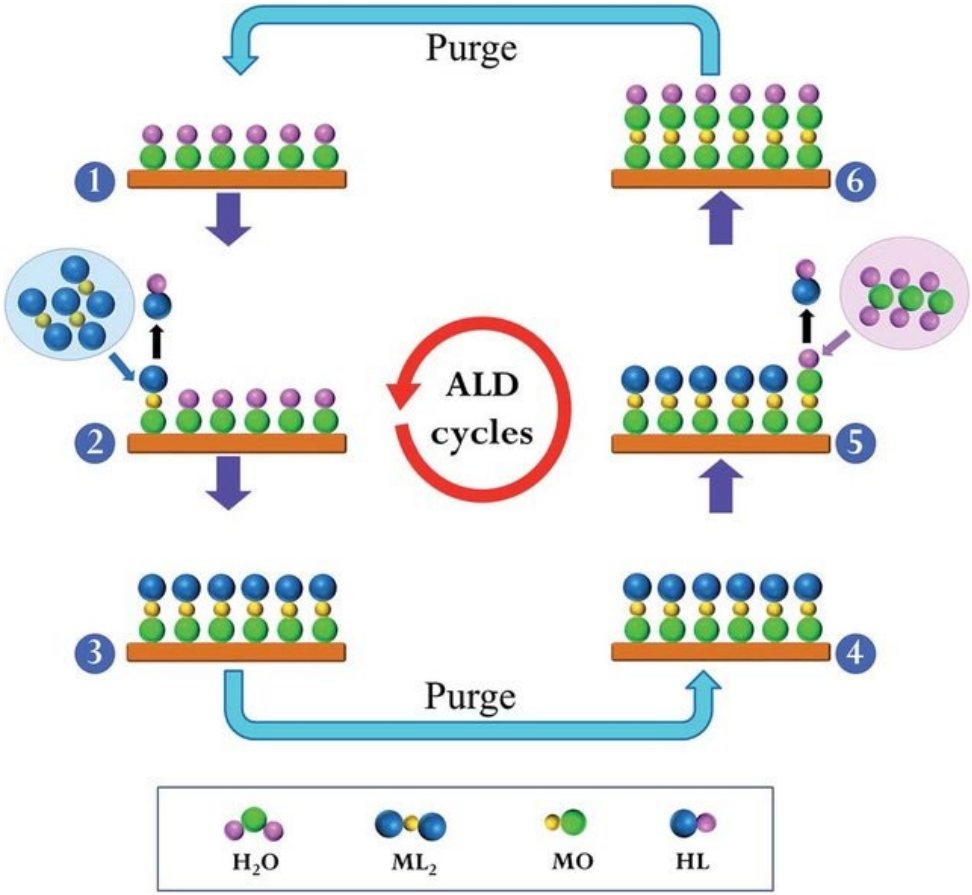
- Wafer is exposed to one or more volatile precursor which react and/or decompose on the substrate surface to produce high quality thin film
- Volatile by-products are removed by gas flow through the reaction chamber
- Materials in various forms: epitaxial, polycrystalline, amorphous
- Materials: Si, SiO2, SiC, SixN, SiON, W, high-k dielectrics, low-k dielectrics
- Several types:
  - By operation conditions: atmospheric, low-pressure (LPCVD), ultrahigh vacuum
  - Plasma methods: plasma-enhanced (PECVD), remote plasma enhanced (RPCVD)
  - By the precursor: metalorganic chemical vapor deposition (MOCVD) etc.



LP CVD

Atomic layer deposition (ALD)

- A subclass of chemical vapor deposition based on subsequential use of gas phase chemical process



Etching techniques

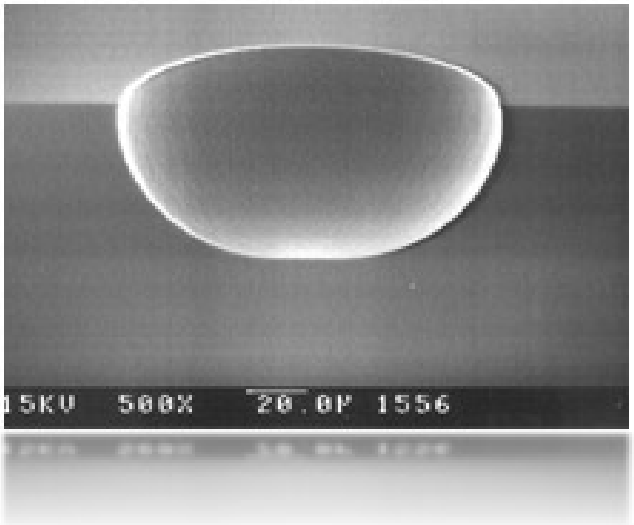
Wet etching

- Liquid etchant
- Chemical reaction
- High selectivity

Dry etching

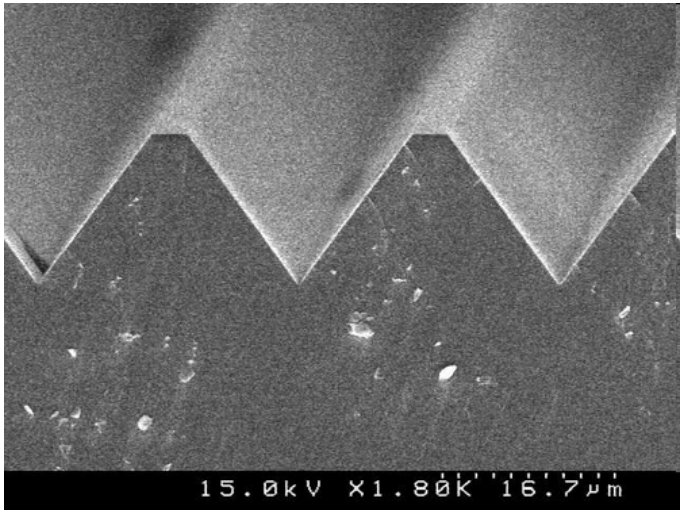
- Vapor phase etchants
- Chemical and physical processes
- Lower selectivity

Isotropic



E.g. HF-HNO_3-CH_3COOH (polishing etchant): etching rate is not direction dependent

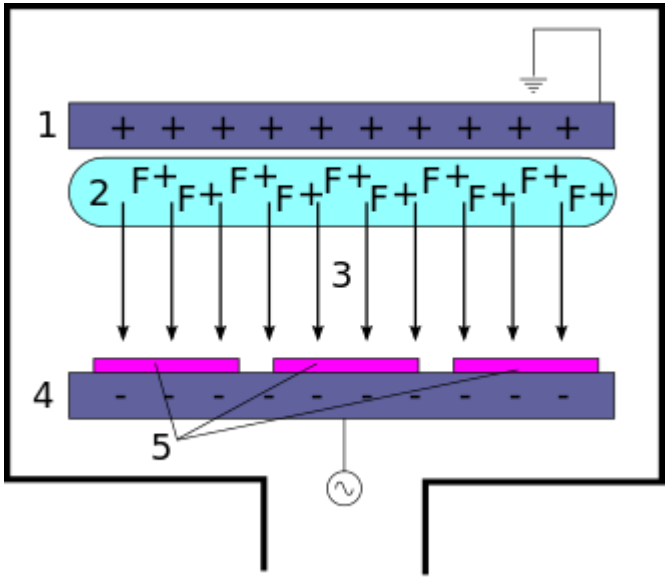
Anisotropic



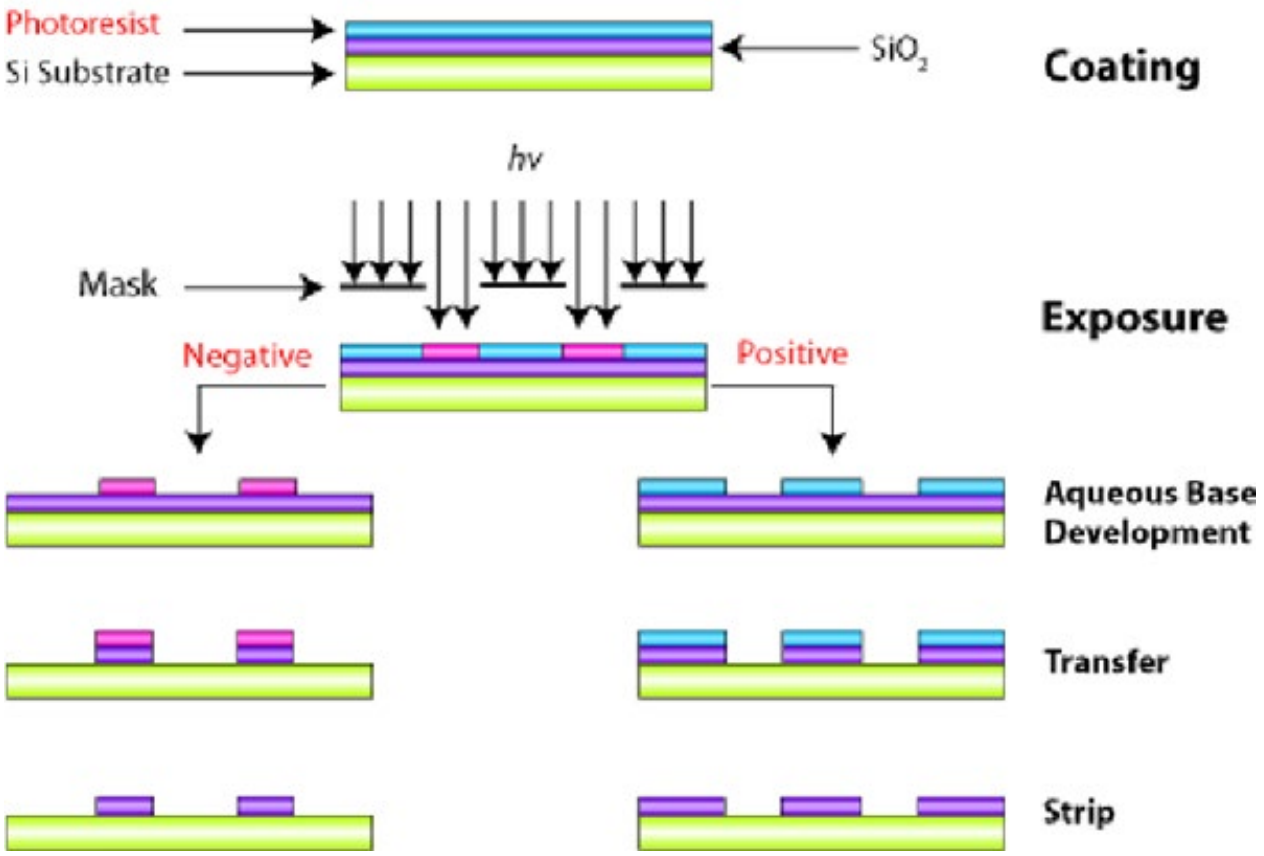
E.g. KOH etch: Etching rate depends on the crystal faces

Reactive ion etching

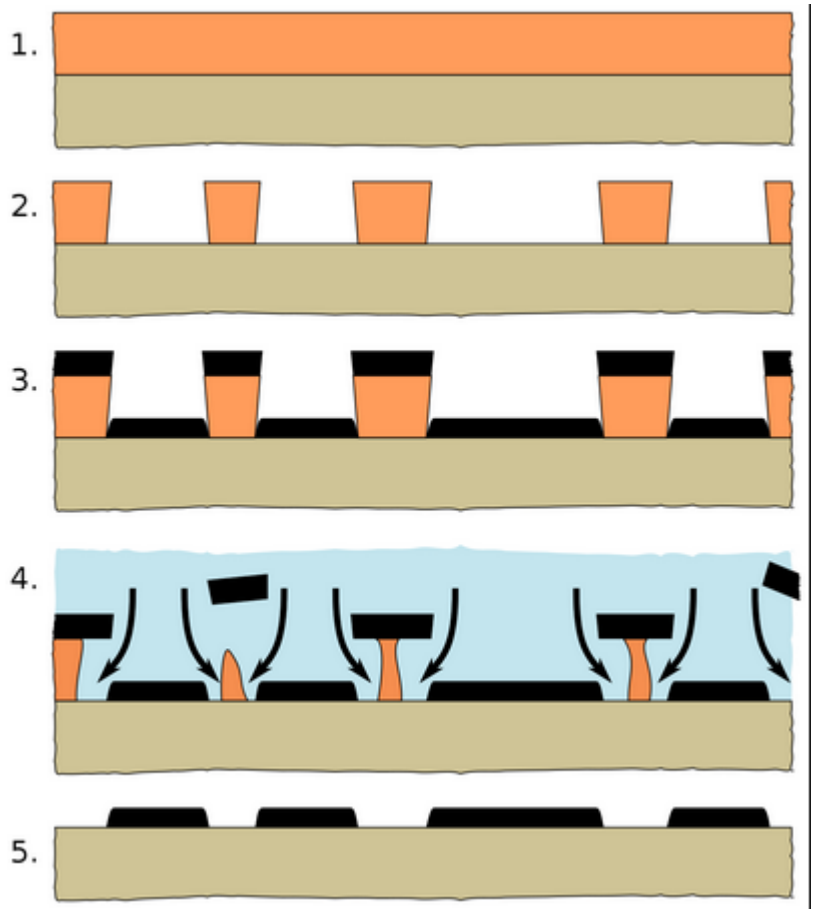
- Chemically reactive plasma to remove materials deposited on the wafer
- Plasma generated in vacuum by an electromagnetic field



Photolithography for etching

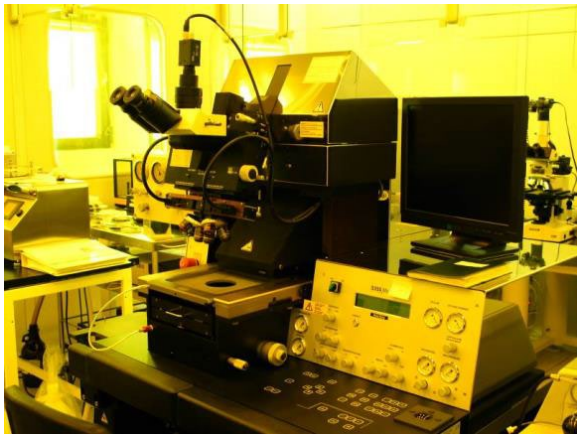


Photolithography for lift-off

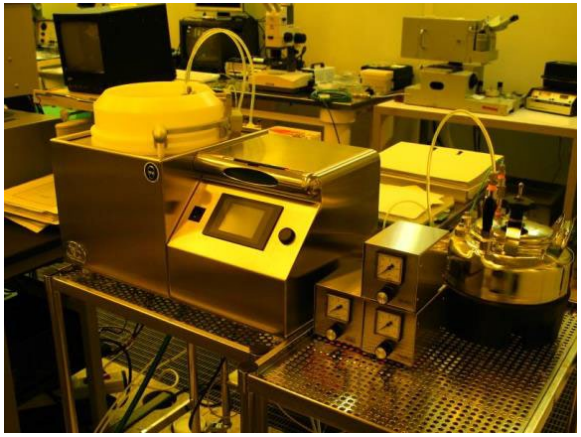


Photolithography

Spin-coater to cover the substrate with photoresist

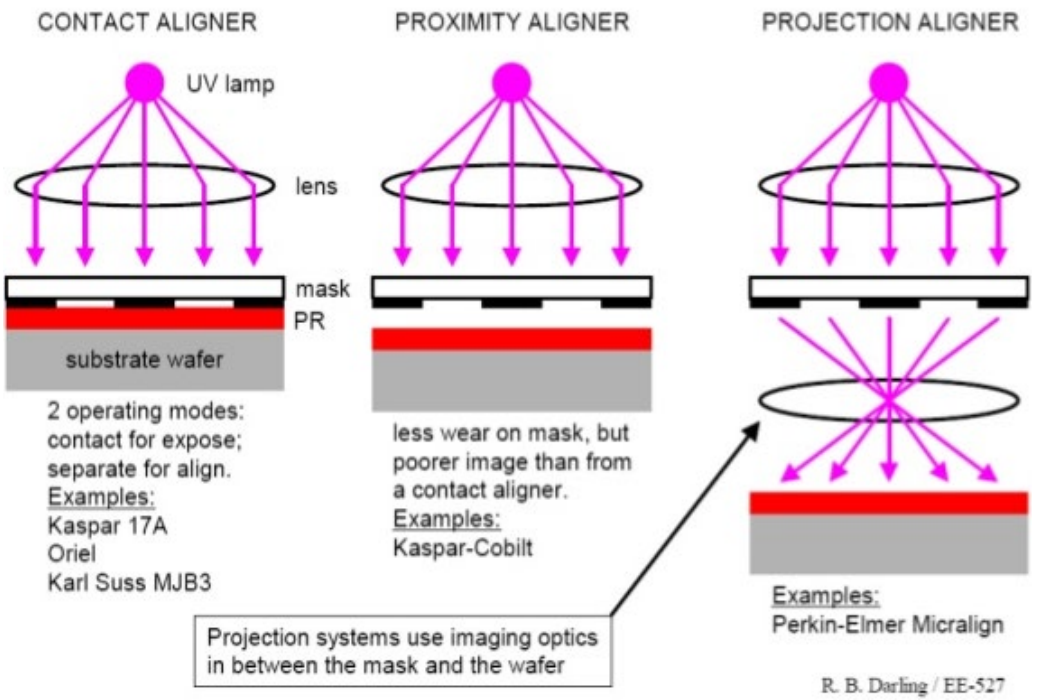


Mask aligner to expose the photoresist through the mask



Developer to remove the exposed photoresist (in case of positive resist)

Photolithography



Critical dimension for projection type:

$$CD = k_1 \frac{\lambda}{NA}$$

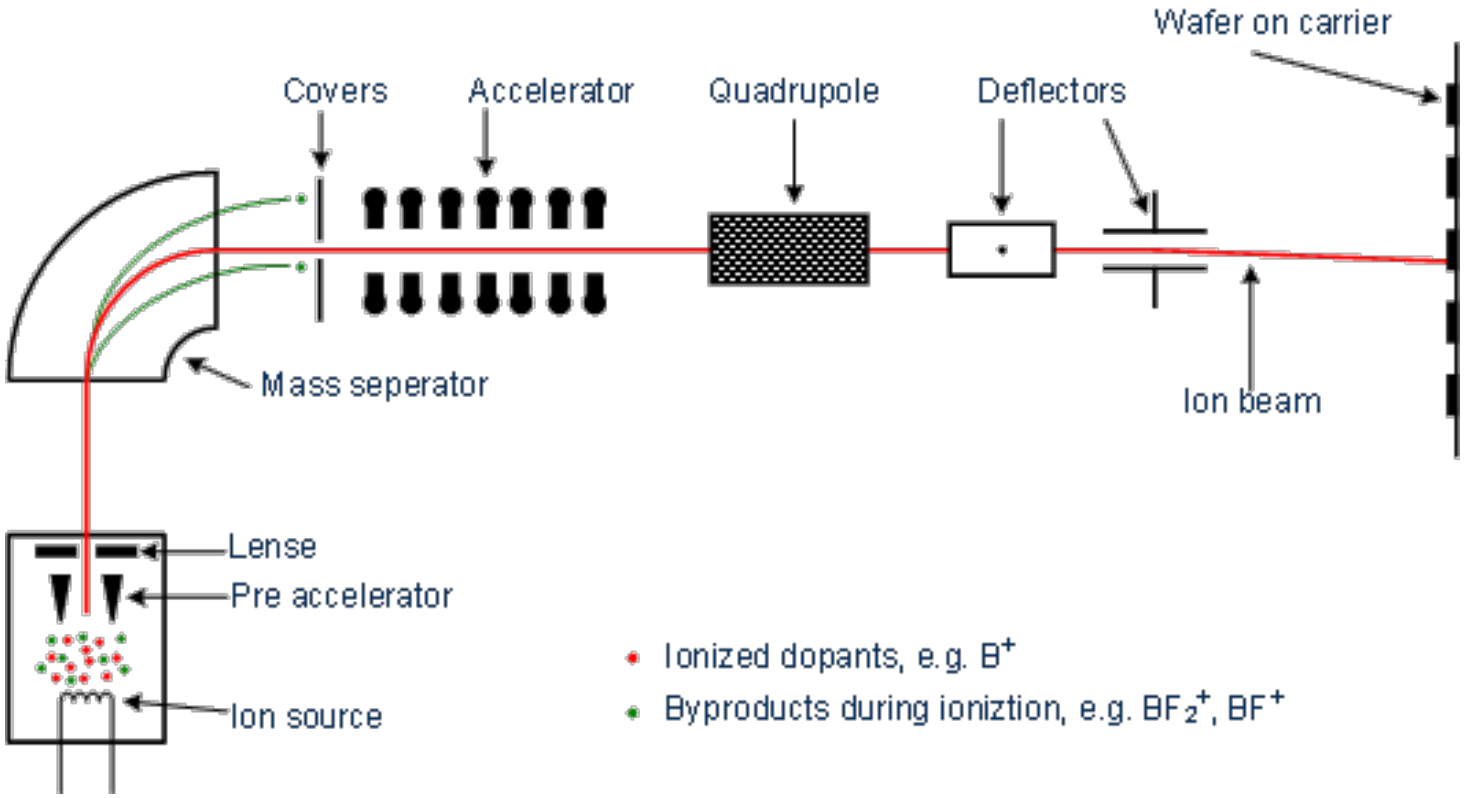
K1: process related factor ~0.4
NA: numerical aperture

Light/UV source:

- Hg lamp: 436 nm (g-line), 405 (h-line), 365 nm (i-line)
- Excimer laser: 248 nm (KrF), 193 nm (ArF); close to the absorption edge of air
- Extreme UV: 13.5 nm

Ion implantation

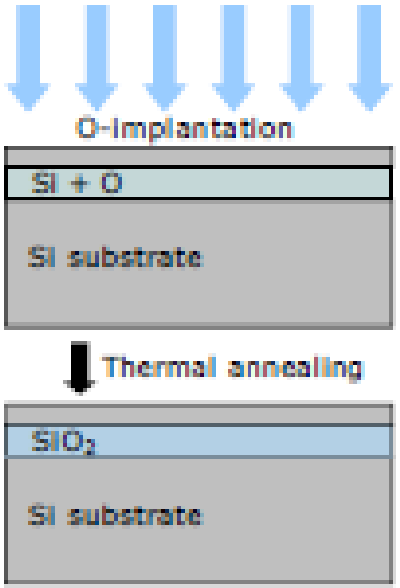
- Ions are accelerated into a solid target for doping (e.g. B for p-type, P for n-type)
- Both kinetic energy and dose can be accurately controlled
- Depth profile can be designed using Monte Carlo simulation (e.g. SRIM)
- Dopants are thermally activated after ion-implantation (substitutional position)



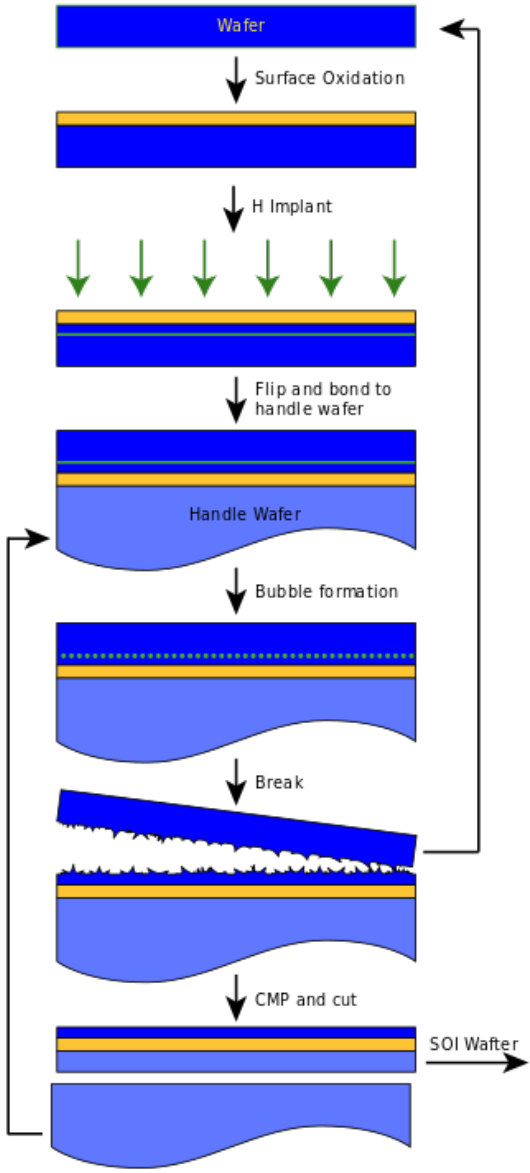
Silicon on Insulator (SOI) wafer

- Thin single crystal Si layer (device) on a buried oxide (BOX)
- To reduce parasitic device capacitance and leakage current
- Also often used for microelectromechanical systems (MEMS): membrane and cantilevers

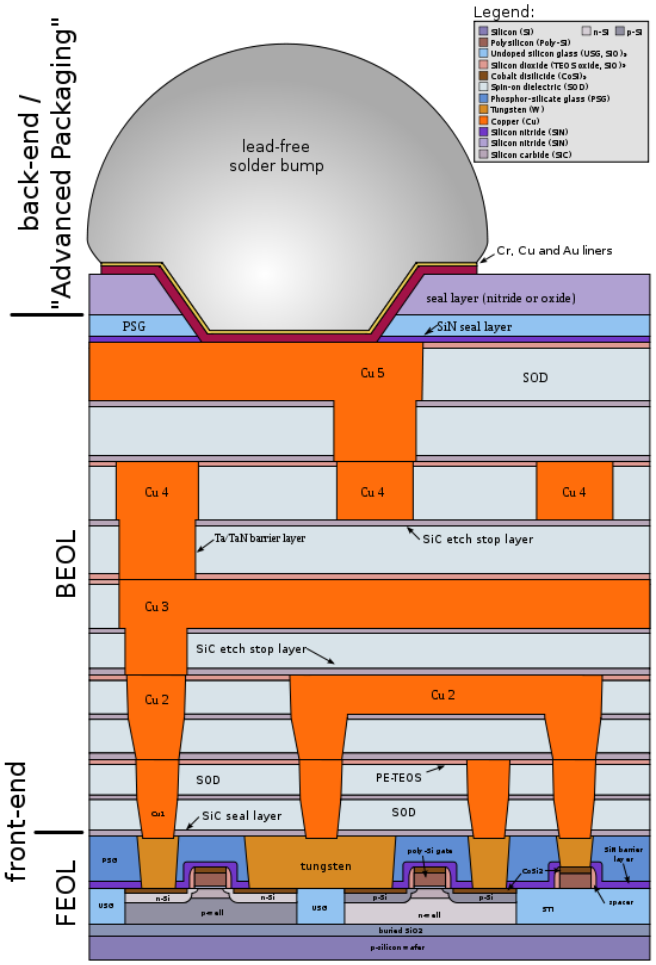
Simox process



Smart cut



Back-end of the line (BEOL) interconnetions



- Traditional IC connectors are made of Al
- Lower resistivity is needed to improve the performance (lower Joule heating, higher current density)
- Challenge with: patterning; doesn't produce volatile byproduct
- Solution: **Damascene process** (introduced by IBM in the 1990s)

Damascene gold plate

Damascene process

Instead of etching the metal via photolithography pattern, gaps in low-k dielectric are filled by PVD seed layer and electroplated Cu.

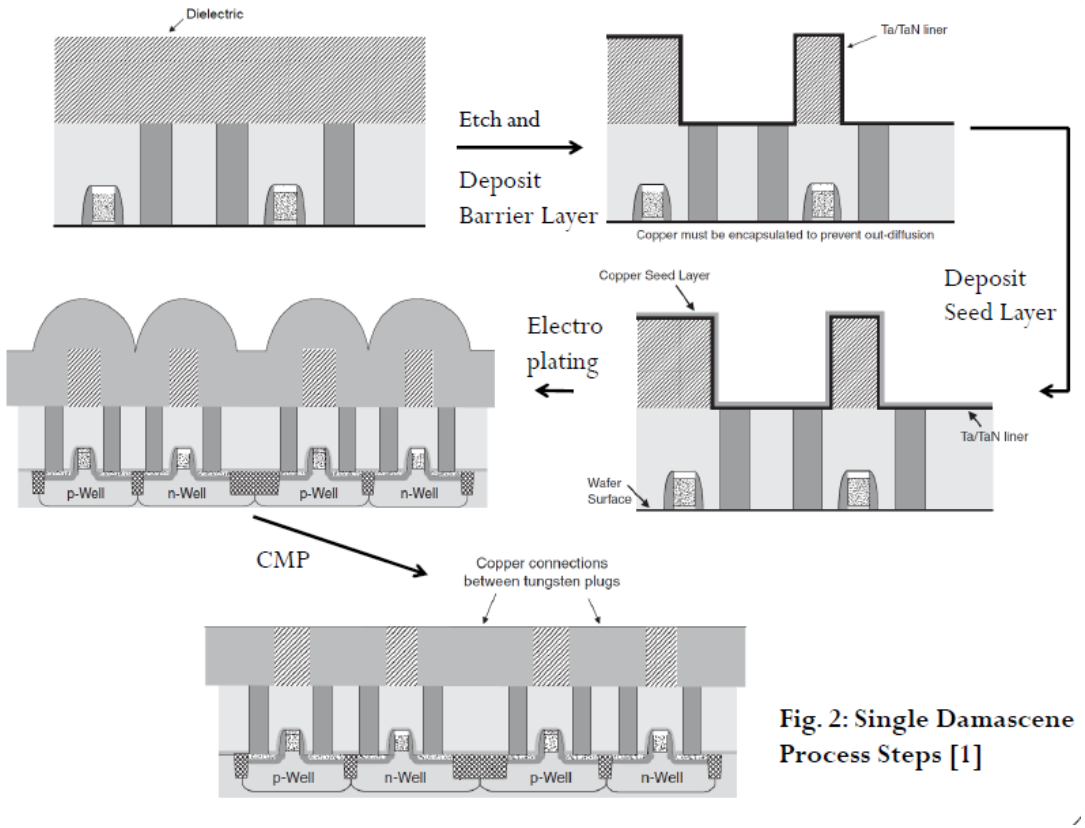
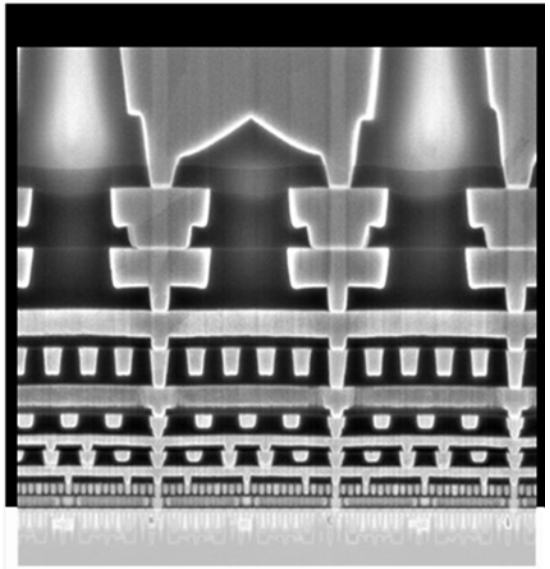


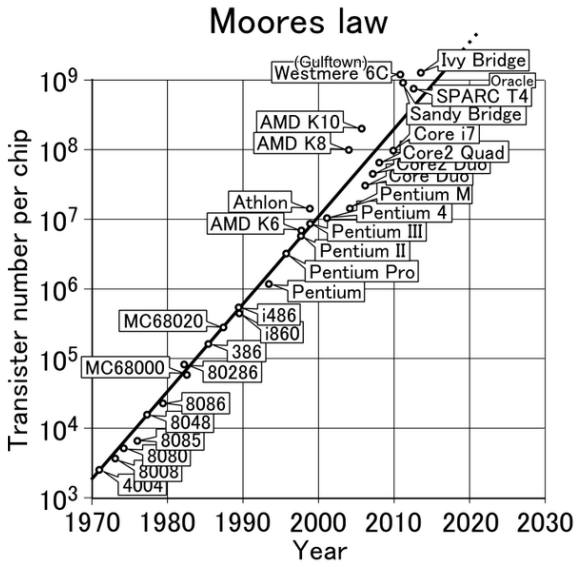
Fig. 2: Single Damascene Process Steps [1]

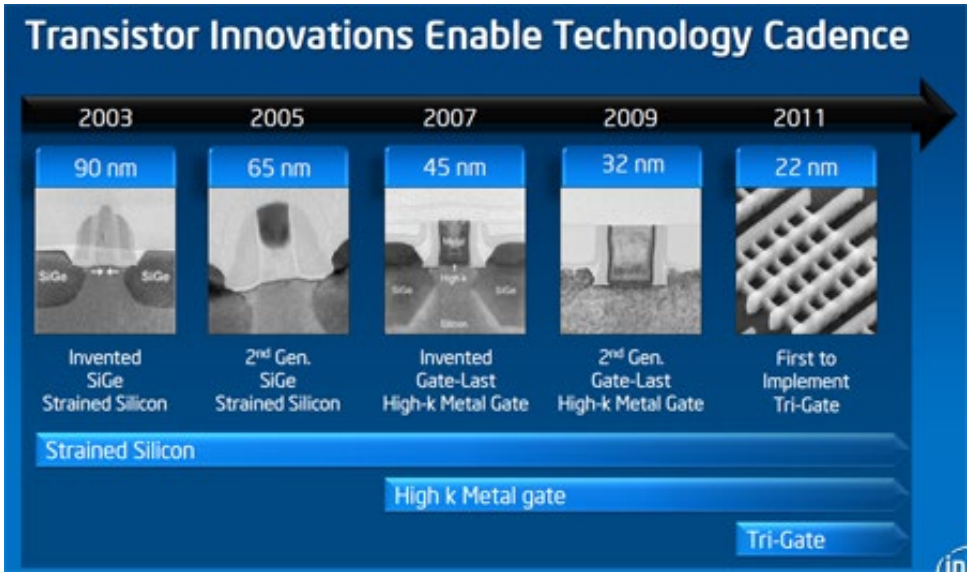
State-of-the-art SRAM



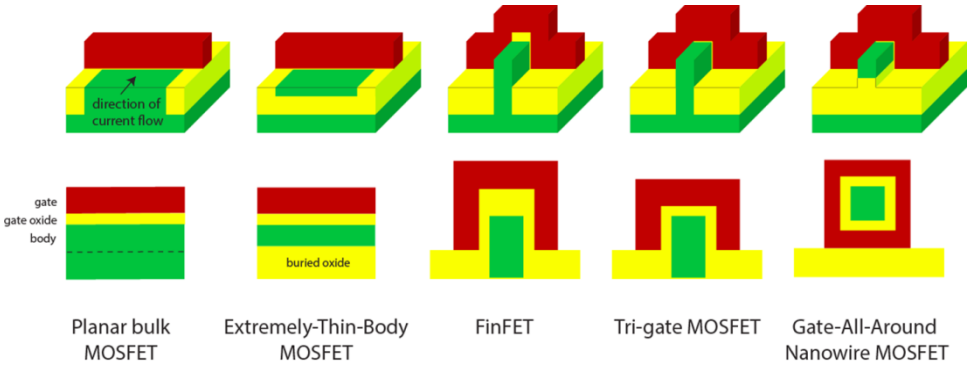
Trends in IC industry

Evolution of the CMOS technology



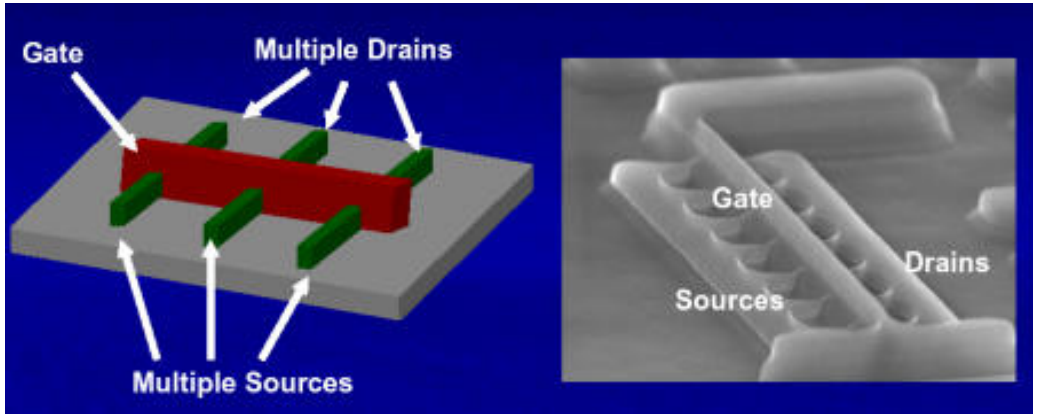


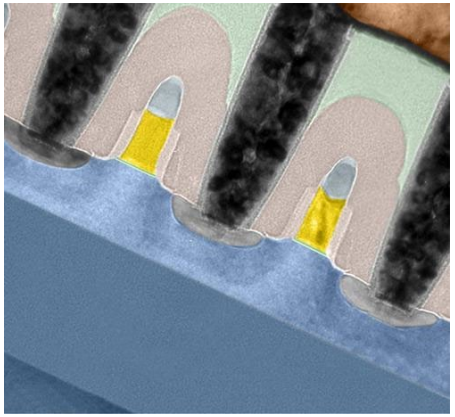
- The progress follows the Moore's law
- Continuously shrinking dimension; currently the state-of-the art node is 16/14 nm
- New transistor architectures emerge: Fin-FET trigate etc.

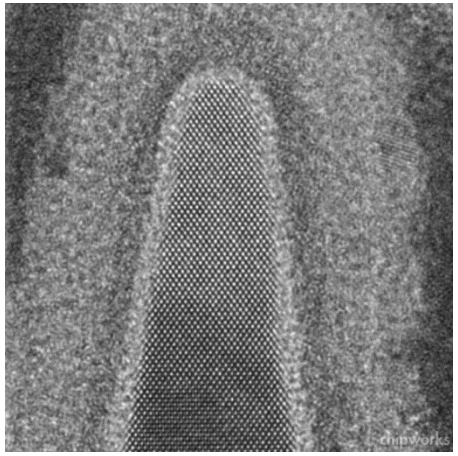


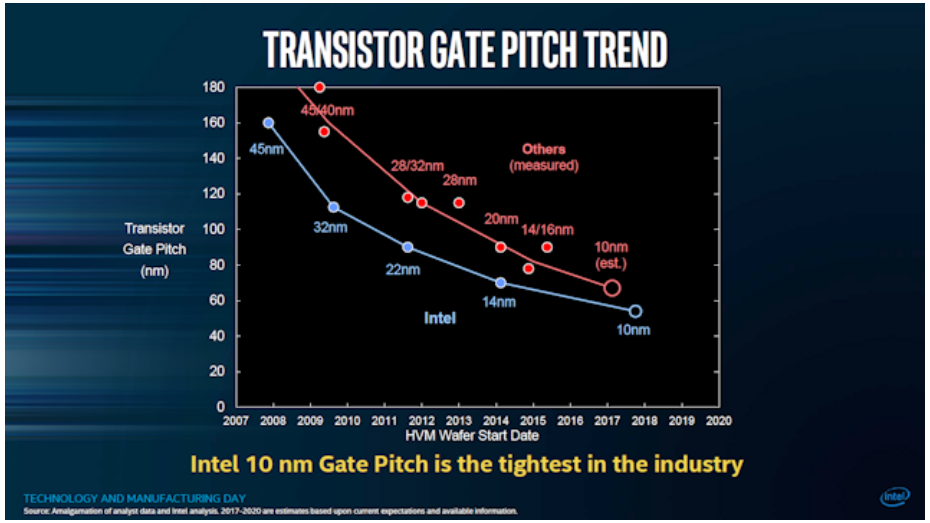
CMOS today

Tri-gate Fin-FET of Intel with 14-nm technology (2014)

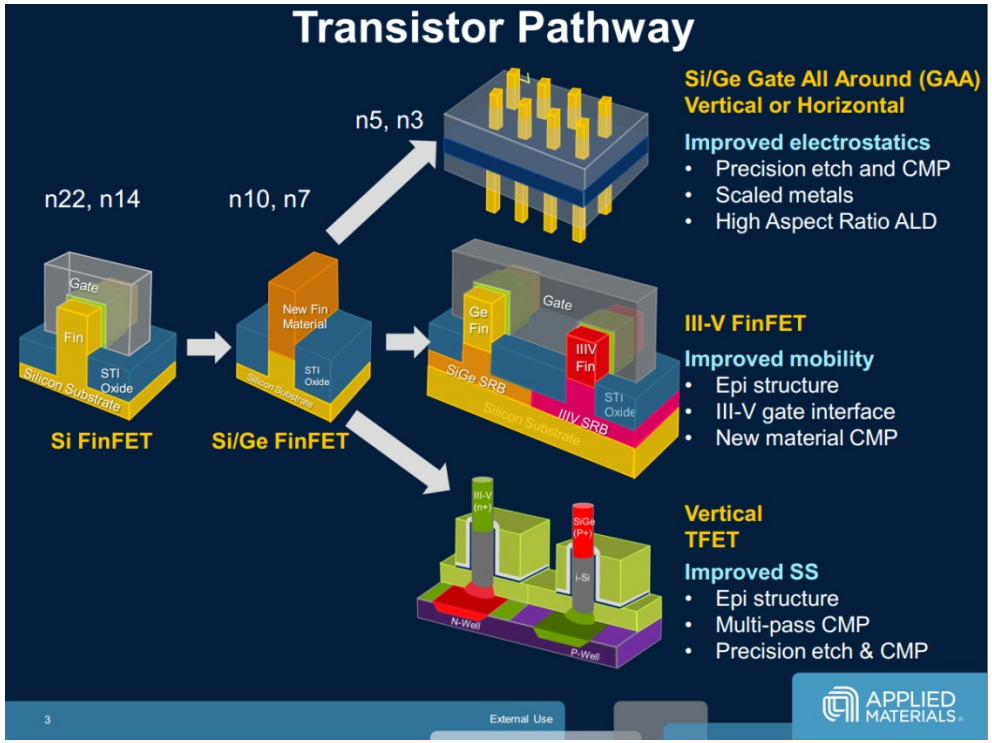


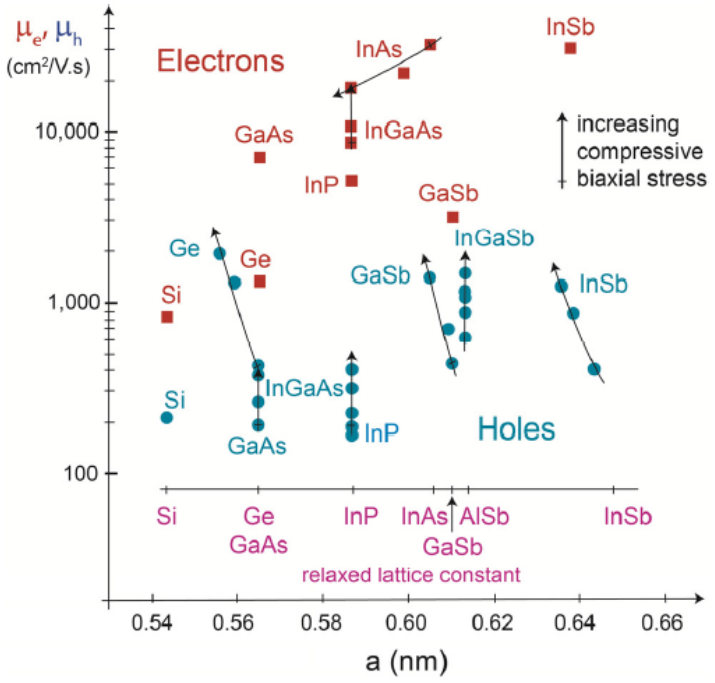






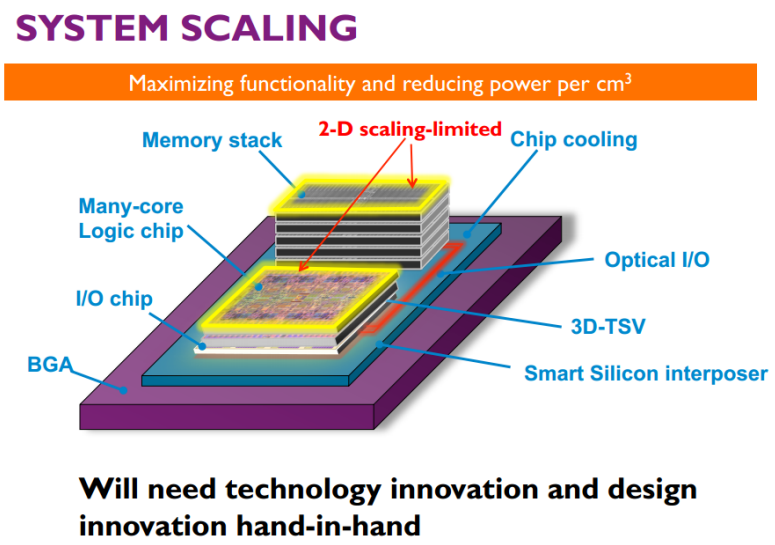
Future of CMOS

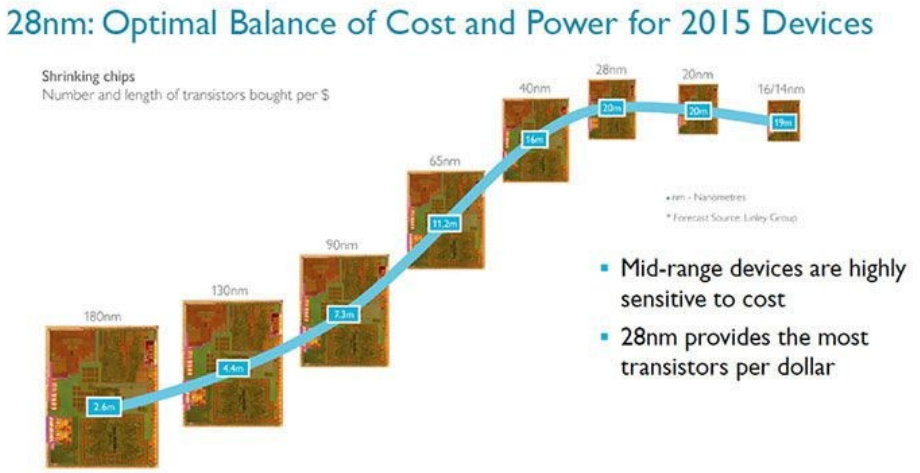




- New device architectures: horizontal and vertical **nanowires (NW)** for gate-all-around (GAA) transistors
- New channel materials beyond Si: Ge-Si or Ge for p-MOS, III-V (InGaAs) for n-MOS (no novel 2D material or CNT on the horizon, yet)

Future of IC technology





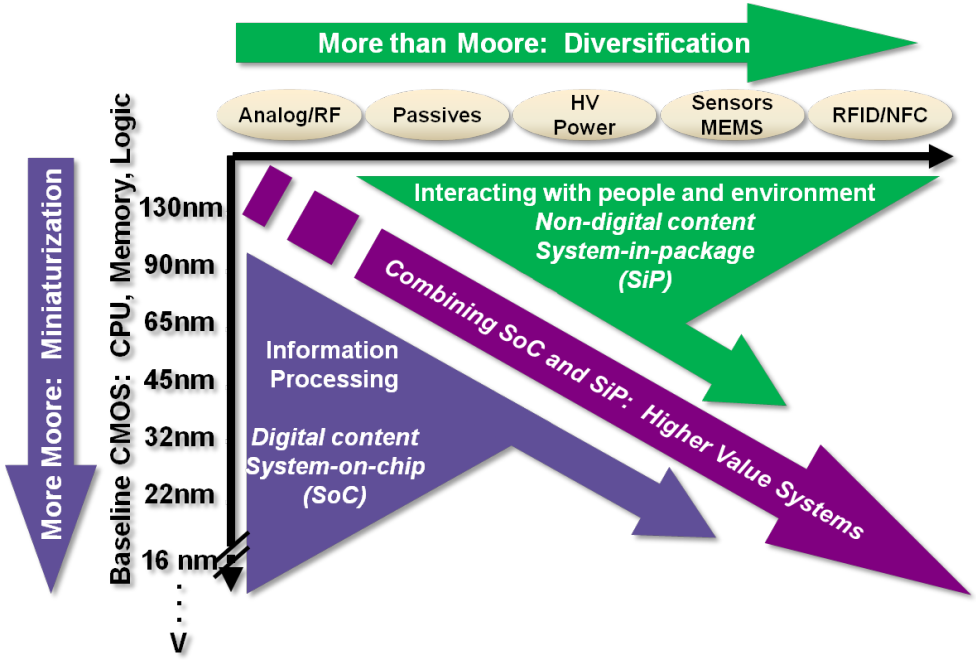
- 3D integration and chip cooling rather than size reduction
- Economical concerns: 450 mm wafer, EUV lithography etc.? Cost per chip does not decrease further.

ASML's EUV lithography machine may eventually look like

More Moore vs. More than Moore

More-than-Moore with new functions

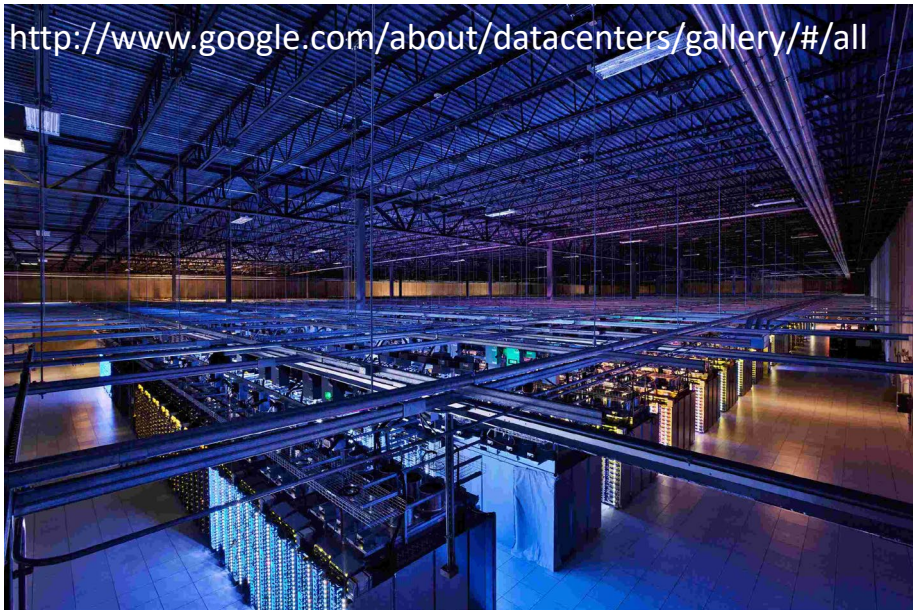
- System-on-chip
- MEMS/NEMS sensors and actuators
- Sheap, printed and flexible electronics, RF ID-s
- Internet of (every) things (IoT), autonomous sensor networks powered by energy harvesters

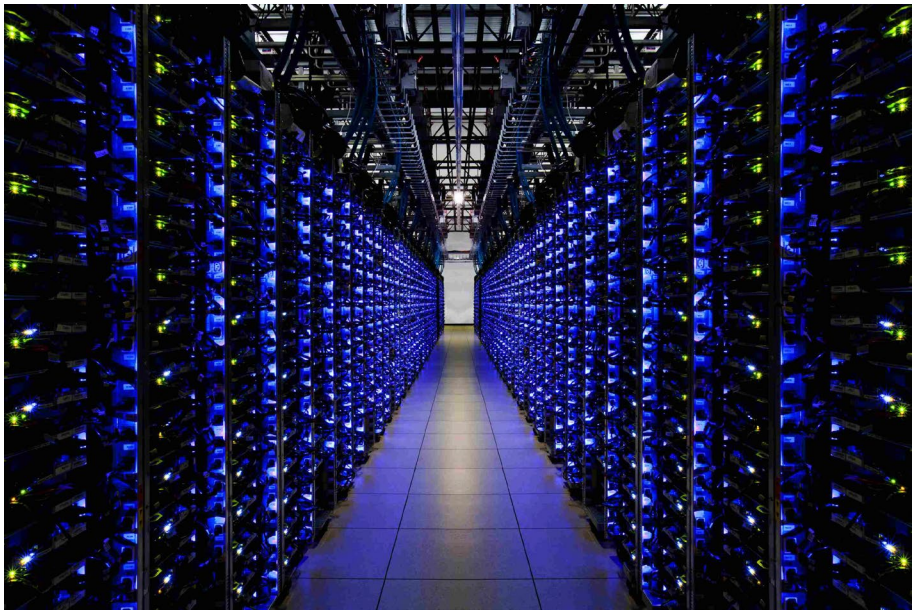


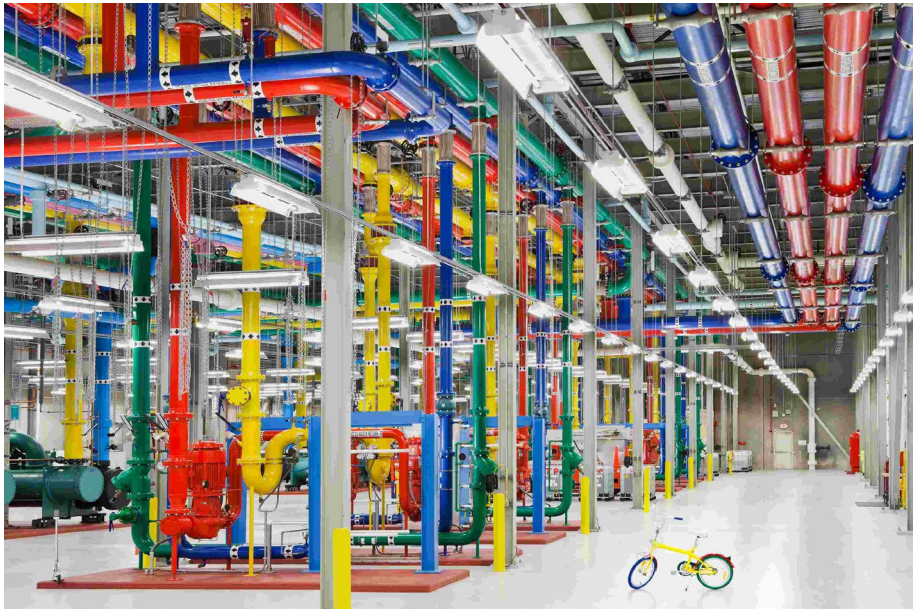
Main challenge of this century where the semiconductor (nanowires) can play a key role: energy!

- Renewable sources: solar cells (Si), energy harvesters for IoT etc.
- Reduce or mitigate the costs: lighting (GaN, 20%), ICT

Energy consumption of ICT >10%







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